

Compal Confidential

EOC20/EOY10

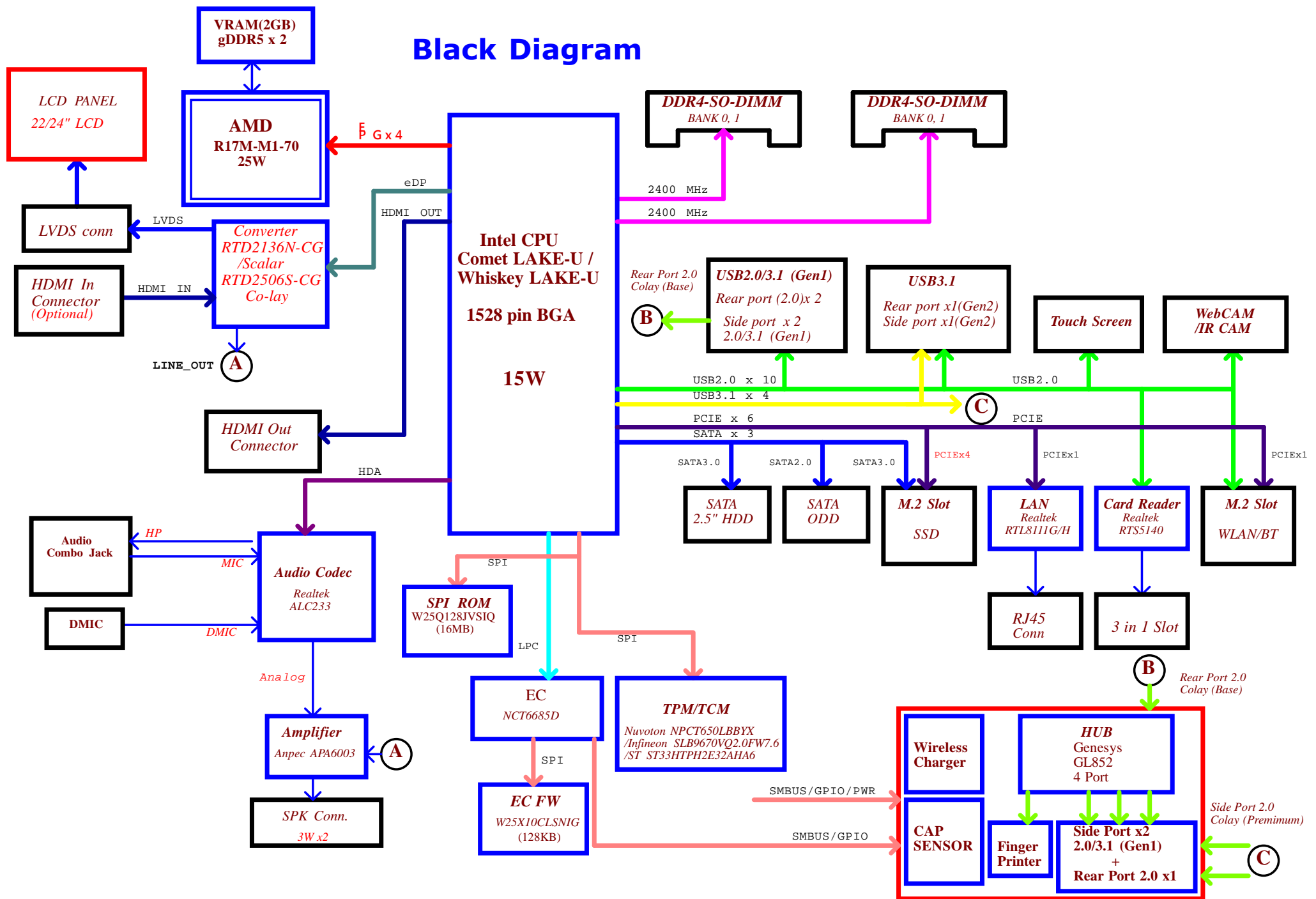
CML-U/WHL-U with R17-M1-70
M/B Schematics Document

LA-H031P

2018-12-04

REV : 1 . 0

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2018/2/5	Deciphered Date	2019/2/5	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Title		Cover Page	
		Size Custom	Document Number		Rev 0.1
		Date:	Tuesday, December 04, 2018		Sheet 1 of 63



Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2015/12/25	Deciphered Date	2016/09/24	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Black Diagram		
Size	Document	Number	Rev	LA-H031P		
Custom			0.1			
Date:	Tuesday, December 04, 2018	Sheet	2	of 63		

PCIe Port Table		
No.	Port	Device
1	5	GPU
2	6	GPU
3	7	GPU
4	8	GPU
5	9	WLAN
6	10	LAN
7	13	SSD
8	14	SSD
9	15	SSD
10	16	SSD

SATA Port Table		
No.	Port	Device
1	11	HDD
2	12	ODD
3	15	SSD
4	16	SSD

DDI Port Table		
No.	Port	Device
1	DDI1	HDMI OUT
2	DDI2	NC

BOARD ID Table	
Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	

USB2.0 Port Table		
Port	Device	OC# Pin
1	JUSB3 (Rear)USB3.0 GEN2	OC#0
2	TOUCH	NA
3	JUSB1 (Rear)	OC#1
4	JUSB6 (Side)USB3.0 GEN2	OC#3
5	JUSB2 (Rear)	OC#1
6	Web Camera	NA
7	Card Reader	NA
8	JUSB4 (Side)Colay USB3.0	OC#2
9	JUSB5 (Side)Colay USB3.0	OC#2
10	WLAN/BT	NA

USB2.0 HUB Port Table (V540)	
Port	Device
1	Co-lay Rear JUSB2
2	Finger Print
3	Colay JUSB4 (Side)
4	Colay JUSB5 (Side)

USB3.0 Port Table		
No.	Port	Device
1	1	USB3.0 (Rear IO) GEN2
2	2	USB3.0 (Side IO) GEN1
3	3	USB3.0 (Side IO) GEN1
4	4	USB3.0 (Side IO) GEN2
5	5	NC
6	6	NC

BOM Structure Table

BOM Structure	BTO Item
PCB	PCB
DC20V	DC20V
RTCVCC_S5	RTCVCC_S5
+3V3_DS	+3V3_DS
+3VALW_S5	+3VALW_S5
+5VALW_S5	+5VALW_S5
+12VALW_S5	+12VALW_S5
+1.8VALW_S5	+1.8VALW_S5
+1.05VALW_S5	+1.05VALW_S5
+1.05V_VCCST_S3	+1.05V_VCCST_S3
+1.2V_VDDQ_S3	+1.2V_VDDQ_S3
+2.5V_S3	+2.5V_S3
+CPU_VCCIO_S0	+CPU_VCCIO_S0
+5VS_S0	+5VS_S0
+3VS_S0	+3VS_S0
+12VS_S0	+12VS_S0
+VCC_SA_S0	+VCC_SA_S0
+VCC_CORE_S0	+VCC_CORE_S0
+VCC_GT_S0	+VCC_GT_S0
+3VS_DGPU_S0	+3VS_DGPU_S0
+VGA_CORE_S0	+VGA_CORE_S0
+1.05VS_DGPU_S0	+1.05VS_DGPU_S0
+1.35VS_VGA_S0	+1.35VS_VGA_S0

Power Plane	Description	S0	S3	S4/S5
+DC20V	AC or battery power rail for power circuit.	N/A	N/A	N/A
+RTCVCC_S5	RTC power	ON	ON	ON*
+3V3_DS	3.3V DS on power rail	ON	ON	ON*
+3VALW_S5	3.3V always on power rail	ON	ON	ON
+5VALW_S5	5V always on power rail	ON	ON	ON
+12VALW_S5	12V always on power rail	ON	ON	ON
+1.8VALW_S5	1.8V always on power rail	ON	OFF	OFF
+1.05VALW_S5	1.05V always on power rail for PCH	ON	ON	ON
+1.05V_VCCST_S3	1.0V power rail for CPU VCCST	ON	ON	OFF
+1.2V_VDDQ_S3	1.2V power rail for DDR4	ON	ON	OFF
+2.5V_S3	2.5V power rail for DDR4	ON	ON	OFF
+CPU_VCCIO_S0	0.95V power rail for CPU VCCIO	ON	OFF	OFF
+5VS_S0	5V switched power rail	ON	OFF	OFF
+3VS_S0	3.3V switched power rail	ON	OFF	OFF
+12VS_S0	12V switched power rail	ON	OFF	OFF
+VCC_SA_S0	power rail for CPU VCCSA	ON	OFF	OFF
+VCC_CORE_S0	VCC Core voltage for CPU	ON	OFF	OFF
+VCC_GT_S0	Core voltage for CPU graphic	ON	OFF	OFF
+3VS_DGPU_S0	3.3V power rail for DIS graphic	ON	OFF	OFF
+VGA_CORE_S0	VCC Core voltage for GPU	ON	OFF	OFF
+1.05VS_DGPU_S0	1.05V power rail for DIS graphic	ON	OFF	OFF
+1.35VS_VGA_S0	1.35V power rail for VRAM	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

SKU ID(Project) Table

SKU (UMA&DIS)		A340 DVT BOM Configure Table	
431AEU38L02	Converter (UMA)	431AEU38L02	Converter (UMA)
X4AEU38L01	Converter (DIS)	X4AEU38L01	Converter (DIS)
431AEU38L03	Converter (DIS)	431AEU38L03	Converter (DIS)
X4AEU38L02	Converter (DIS)	X4AEU38L02	Converter (DIS)
431AEU38L04	Converter (DIS)	431AEU38L04	Converter (DIS)
X4AEU38L02	Converter (DIS)	X4AEU38L02	Converter (DIS)
431AEU38L05	Converter (DIS)	431AEU38L05	Converter (DIS)
X4AEU38L02	Converter (DIS)	X4AEU38L02	Converter (DIS)

SKU ID(Project) Table

SKU (UMA&DIS)		V540 DVT BOM Configure Table	
431AEU38L51	Scalar (UMA)	431AEU38L51	Scalar (UMA)
X4AEU38L51	Scalar (DIS)	X4AEU38L51	Scalar (DIS)
431AEU38L52	Scalar (UMA)	431AEU38L52	Scalar (UMA)
X4AEU38L51	Scalar (DIS)	X4AEU38L51	Scalar (DIS)

Voltage Rails

PCH SM Bus Address

Device	Address	HEX
DDR(JDIMM1)	WRITE:0xA0	READ: 0xA1
DDR(JDIMM2)	WRITE:0xA4	READ: 0xA5

EC SM Bus2 Address

Device	Address	HEX
Scalar	x	x
LCD Backlight	0110-0010xb	62

EC SM Bus0 Address

Device	Address	HEX
Converter	1001-0100xb	94
GPU	1000-0010xb	82
PCH	1001-0000xb	90
Thermal	1001-1010xb	9A

G3->S0

S0->S3/DS3

S0/DS3->S0

S0->S5

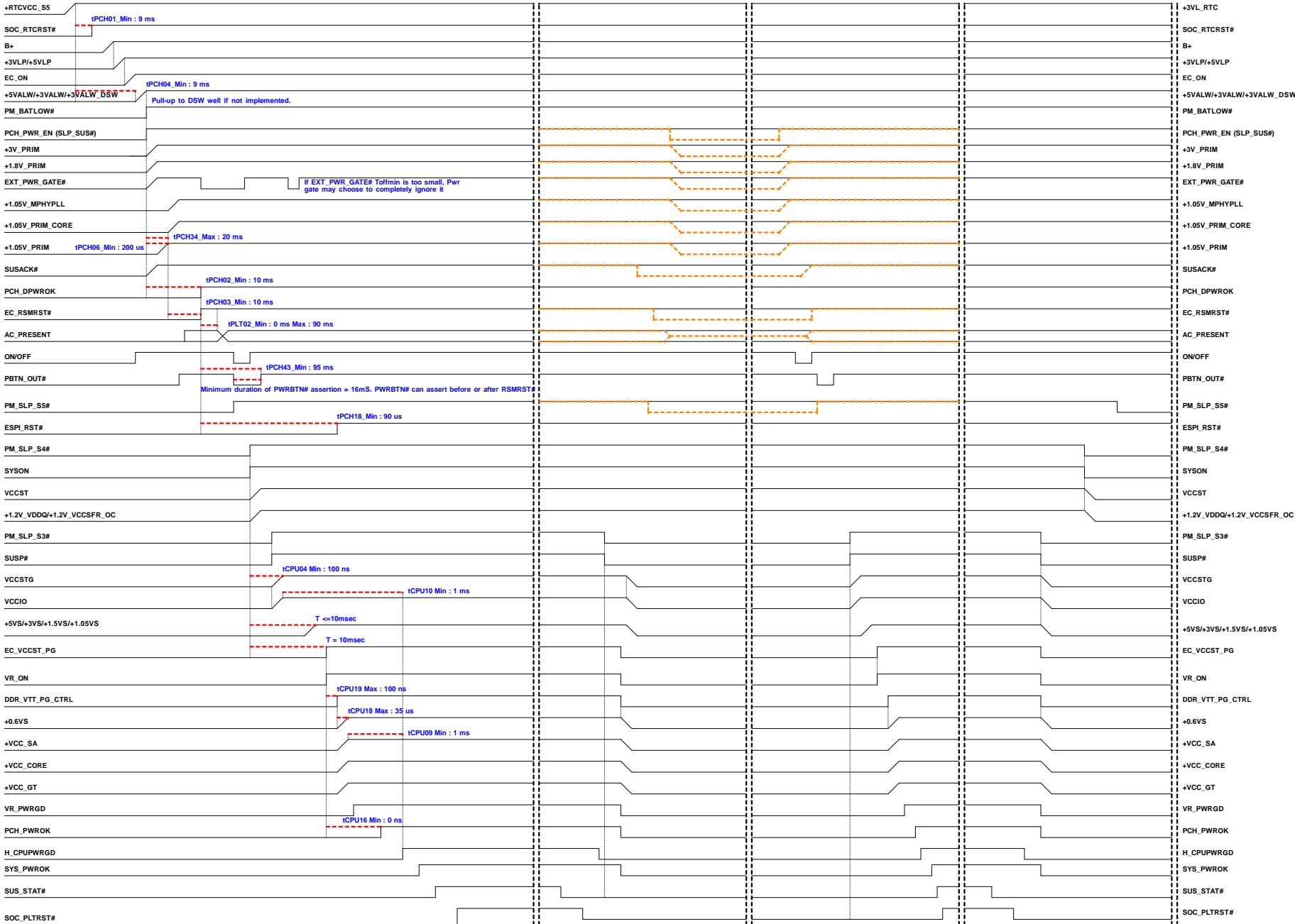
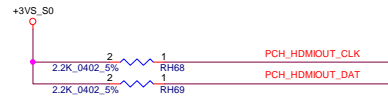


Table 5-13. DDI Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm $\pm 5\%$ resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm $\pm 5\%$ resistor	
Port 3	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm $\pm 5\%$ resistor	
Port 4	DDPF_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm $\pm 5\%$ resistor	



< Compensation PU For eDP >

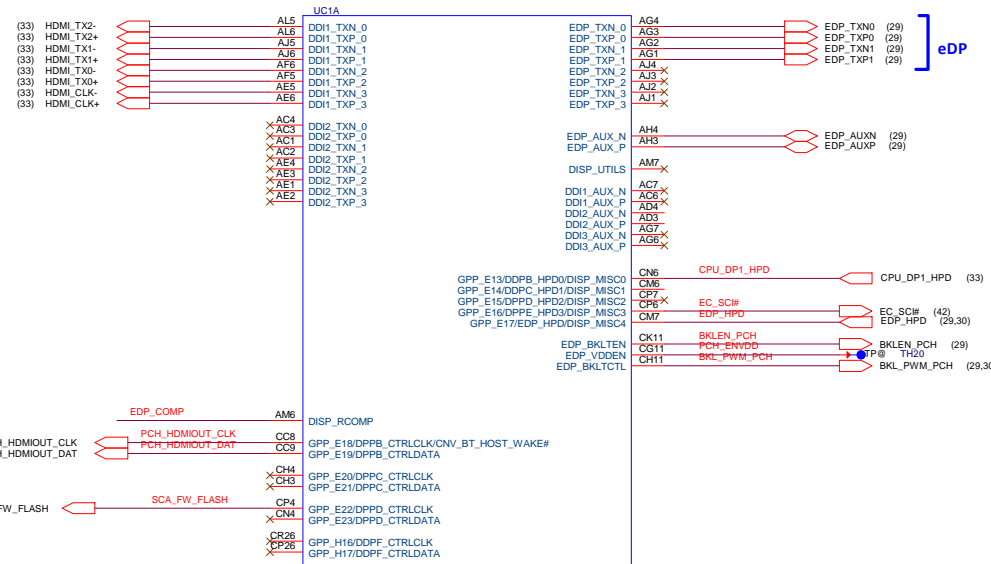
+CPU_VCCIO_S0

RC9 1 2 24.9_0402_1% EDP_COMP

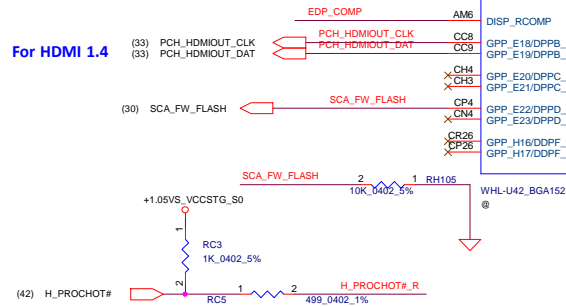
Trace width=5 mils, Spacing=25mil, Max length=600mils

1009 : Remove RCOMP option

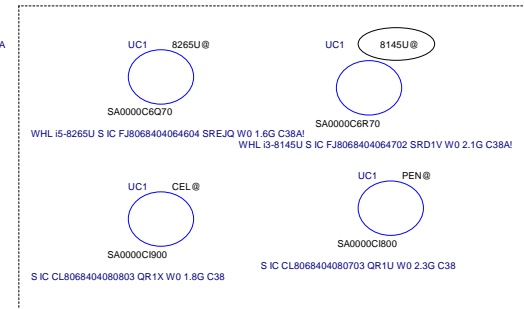
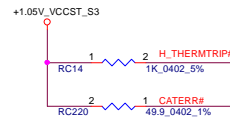
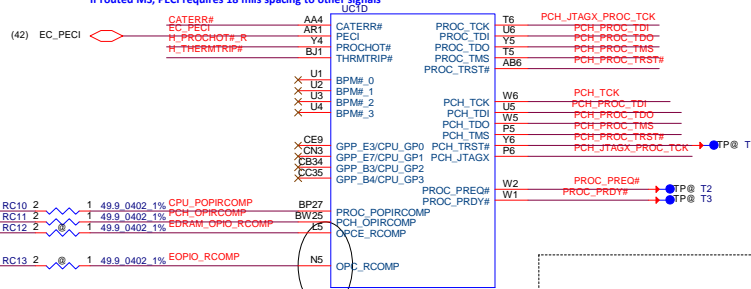
HDMI



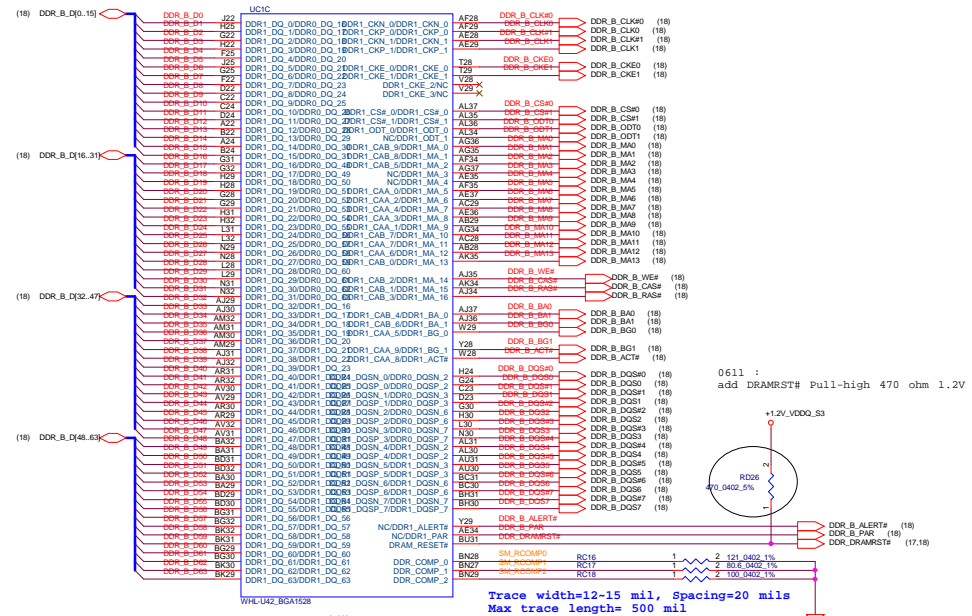
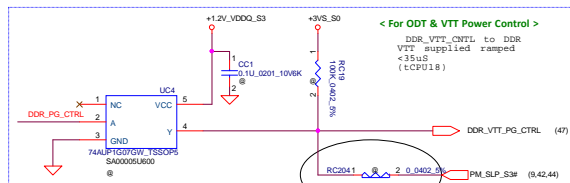
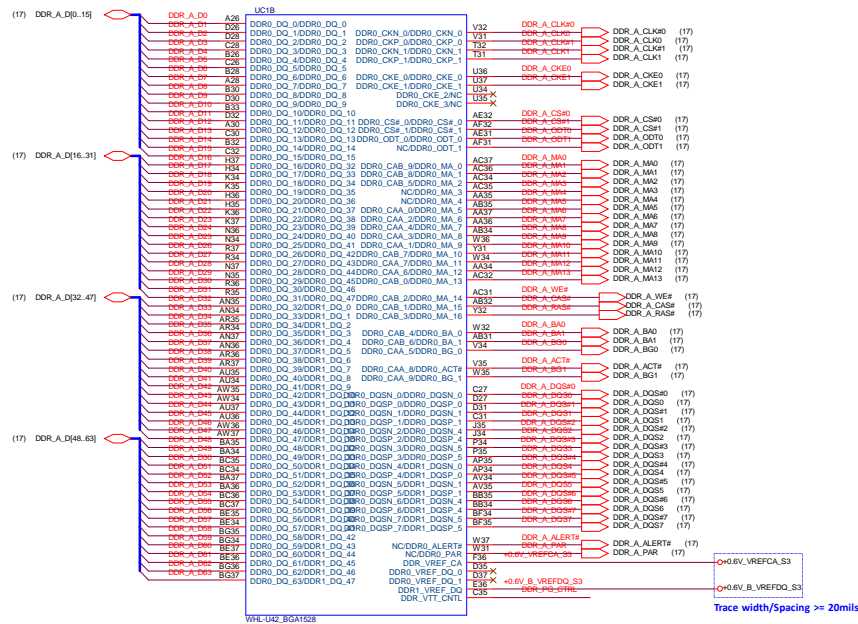
For HDMI 1.4



If routed MS, PECO requires 18 mils spacing to other signals



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/5/3	Deciphered Date	2017/6/2	Title	WHL-U(1/12)DDI,EDP,MISC,CMC
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Rev
				Custom LA-H031P	0.1
Date:		Tuesday, December 04, 2018		Sheet	5 of 63



RCOMP Recommendation for WHL and CFL

Interface	Pin Name	Board Rterm (Ohm)	Board Rdc (Ohm)
DDR - DDR4 SODIMM	DDR_RCOMP[0]	1210 ±1% on plg to VSS	N/A
	DDR_RCOMP[1]	80.60 ±1% on plg to VSS	N/A
	DDR_RCOMP[2]	1002 ±1% on plg to VSS	N/A

RCOMP Recommendation for CNL

Interface	Pin Name	Board Rterm (Ohm)	Board Rdc (Ohm)
DDR - DDR4 SODIMM	DDR_RCOMP[0]	1002 ±1% on plg to VSS	N/A
	DDR_RCOMP[1]	1002 ±1% on plg to VSS	N/A
	DDR_RCOMP[2]	1000 ±1% on plg to VSS	N/A

Trace width=12-15 mil, Spacing=20 mils
Max trace length= 500 mil

1009 : Remove RCOMP option

Security Classification	Compal Secret Data	Issued Date	Deciphered Date	2020/5/17	Title	WHL-U(2)DDR4
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSMITTED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						Rev 0.1
Date: Tuesday, December 04, 2018						Sheet 6 of 63













The image contains two circuit diagrams, each enclosed in a dashed rectangular box. Both diagrams show a 3V supply connected to a resistor network.

Left Diagram:

- A red circle at the top is labeled **+3VALW_S5**.
- A red wire connects this circle to a blue resistor labeled **RC224** and **10K_0402_5%**.
- The other end of RC224 is connected to a red wire labeled **TPM@**.
- A red wire labeled **TPM_MODE** is connected to a red dot on a red wire that runs horizontally across the diagram.
- Below this horizontal wire, a blue resistor labeled **RC226** and **10K_0402_5%** is connected between the horizontal wire and a red wire labeled **SW_TPM@**.
- At the bottom, a red wire is connected to a red triangle symbol.

Right Diagram:

- A red circle at the top is labeled **+3VALW_S5**.
- A red wire connects this circle to a blue resistor labeled **RC225** and **10K_0402_5%**.
- The other end of RC225 is connected to a red wire labeled **A340@**.
- A red wire labeled **A340_V5_SEL** is connected to a red dot on a red wire that runs horizontally across the diagram.
- Below this horizontal wire, a blue resistor labeled **RC227** and **10K_0402_5%** is connected between the horizontal wire and a red wire labeled **V5@**.
- At the bottom, a red wire is connected to a red triangle symbol.

(37) SOC_SPI_0_CLK  SOC_SPI_0_CLK RC231 1  2 0 0402 5% SPI0_CLK CF
 (37) SOC_SPI_0_SO  SOC_SPI_0_SO RC232 1  2 0 0402 5% SPI0_MISO CF
 (37) SOC_SPI_0_SI  SOC_SPI_0_SI RC233 1  2 0 0402 5% SPI0_MOSI CF
 SW_TPM@  SOC_SPI_0_IO2 CF
 SOC_SPI_0_IO3 CF
 SOC_SPI_0_CS#0 CF
 SOC_SPI_0_CS#2 CF
 3VALW_S5  SOC_SPI_0_CS#2 CF
 RC20 1  2 100K 0201 5% SOC_SPI_0_SI CF
 RC21 1  2 100K 0201 5% SOC_SPI_0_IO2 CF
 RC22 1  2 100K 0201 5% SOC_SPI_0_IO3 CF
 (37) TPM_STSRQ#  TPM_MODE CF
 A340_V5_SEL CF

```
0627: RC26/RC28/RC29/RC31/RC33 change to 51 ohm
      Add RC230 on SOC_SPI_0_CS#0
      RC26,RC28,RC29,RC31,RC33,RC230 need close to UC1
```

< SPI ROM - 16M >

[illegible]

1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.







NOTE: CS# does not need series resistor

1. R1 resistor should be stuffed with 50 ohm for 3.3V and 15 ohm for 1.8V. R1 is not required for CS# signal.
2. S number of vias can be allowed.
3. Continuous ground referencing plane
4. Design guidelines are applies for SPI0_IO2, SPI0_IO3, SPI0_MOSI, SPI0_MISO, SPI0_CLK, SPI0_CS0#, SPI0_CS1# and SPI0_CS2#
5. Design guideline support up to 50MHz
6. R2 resistor should be stuffed with 5 ohm for 3.3V and 1.8V. R2 resistor is not required for CS# signal.

SOC_SMBALERT# RC2151 2 4.7K 0402 5%

SOC_SML0ALERT# RC2161 2 4.7K 0402 5%

SML1
(Link to EC,DGPU)

_SMB_CK0	RC27	1		2	1K_0402_5%
_SMB_DA0	RC30	1		2	1K_0402_5%
_DC_SML1ALERT#	RC32	1		2	150K_0402_5%
_DC_SML0CLK	RC36	2		1	1K_0402_5%
_DC_SML0DATA	RC37	2		1	1K_0402_5%
_CLKRUN#	RC38	1		2	8.2K_0402_5%

The schematic diagram illustrates the PM-SMB bus connection. It features three voltage sources: +3VALW_S5, +3VS_S0, and +3VS_S0. Each source is connected to a resistor (RH18, RH19, RH20, RH24) which is then connected to the PM-SMBCLK and PM-SMBDAT lines. The PM-SMBCLK line is connected to PCH_SMBCLK (17,18) and the PM-SMBDAT line is connected to PCH_SMBDAT (17,18). Two 2N7002KDW_SOT363-6 MOSFETs are shown, with their gates connected to the PM-SMBCLK line and their drains connected to the PM-SMBDAT line. A link to the DDR is indicated.

Security Classification		Compal Secret Data		Compal Electronics, Inc. WHL-U(3/12)SPI,SMB,LPC,ESPI		
Issued Date	2017/5/3	Deciphered Date	2017/6/2	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				Custom		0.1
				Date:	Tuesday, December 04, 2018	Sheet 7 of 63

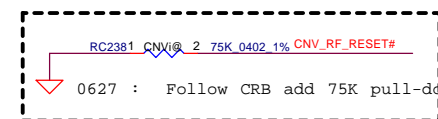
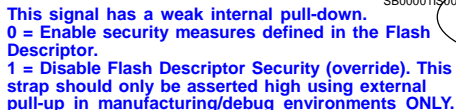


```

To Enable ME Override >
1st source : BSS138W_PANJIT (SB00000T000)
2st source : LBSS139WT1G_LRC (SB00001G000)
0605: QC1 -> PMOS

```

RC202

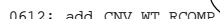


7 of 20

GPP H21 XTAL frequency selected.

0: 38.4/19.2Mhz

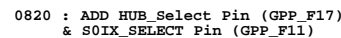
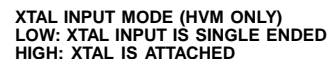
1: 24MHz XTAL selected



0621: COEX1~3 change to test point only



1 = Enable TOP Swap Mode.



Security Classification		Compal Secret Data		Compal Electronics, Inc. WHL-U(4/12)HDA,EMMC,SDIO,CSI2	
Issued Date	2017/5/3	Deciphered Date	2017/6/2	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Rev
				Custom	0.1
				Document Number LA-H031P	
Date: Tuesday, December 04, 2018				Sheet	8 of 63

GPIO_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. ==> Default

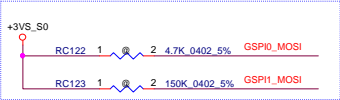
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is used when running ITP/XDP.

GPIO1_MOSI (Internal Pull Down):

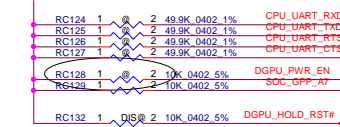
Boot BIOS Strap Bit

0 = SPI Mode ==> Default

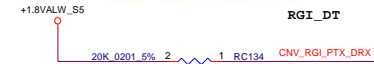
1 = LPC Mode



0627 : Follow CRB reserve 20K pull-up to 1.8VALW

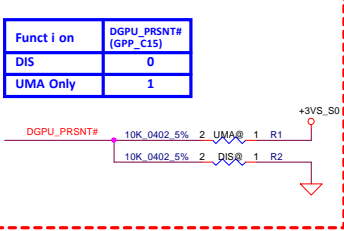
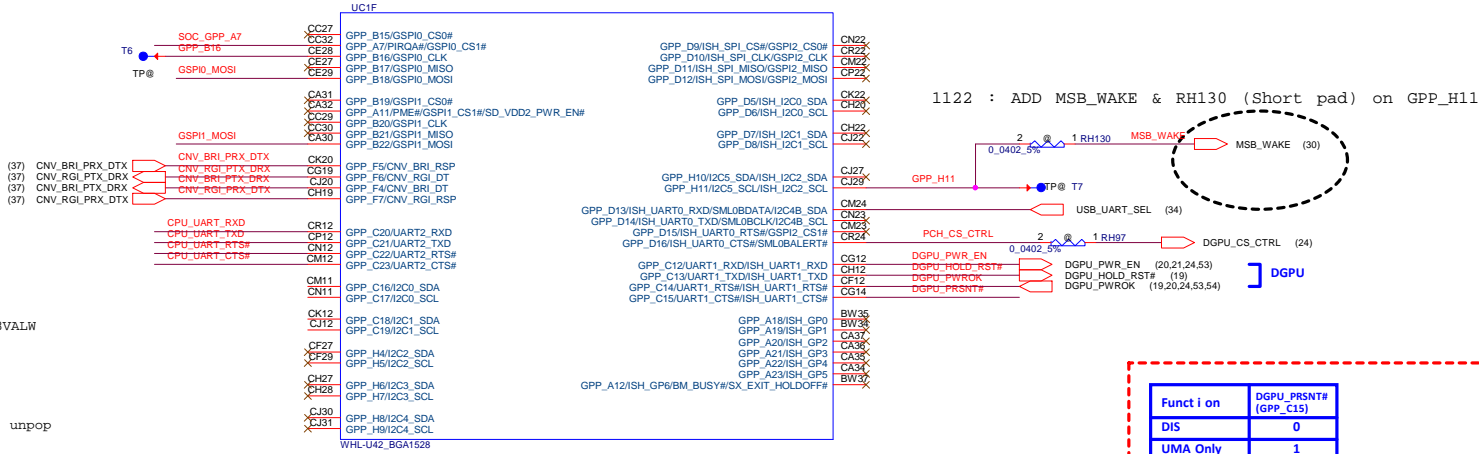


M.2 CNVi MODES
 LOW-> INTEGRATED CNVi ENABLE
 HIGH-> INTEGRATED CNVi DISABLE
 WEAK INTERNAL PU



Place close to PCH

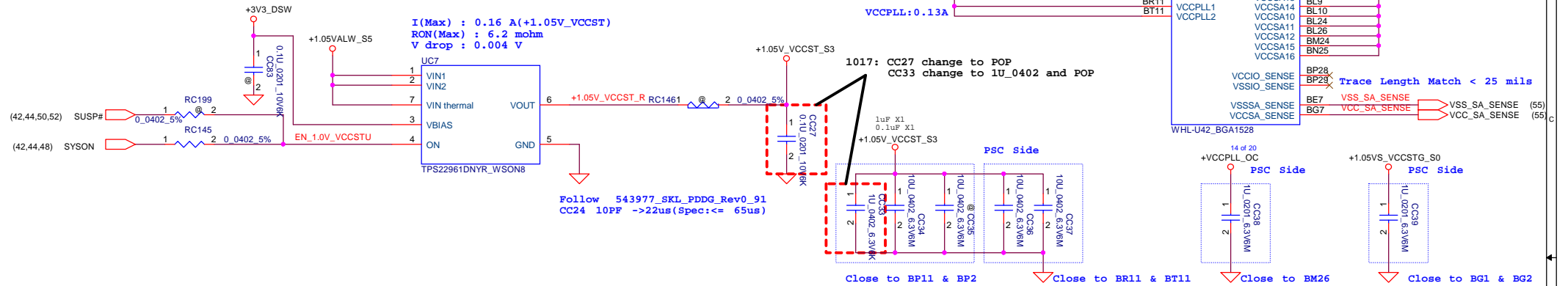
Note: When a RF companion chip is connected to the PCH CNVi interface, the device internal pulldown resistor will pull the strap load to enable CNVi interface.



0615: divide 1.8VS/VCCST switch

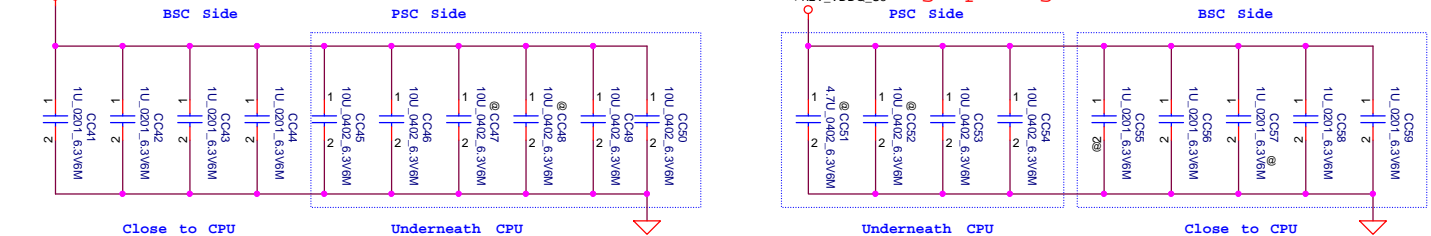
+1.05VALW TO +1.05V_VCCST

0822 : RC146 change to short pad



change package of 1U from 0201 to 0402

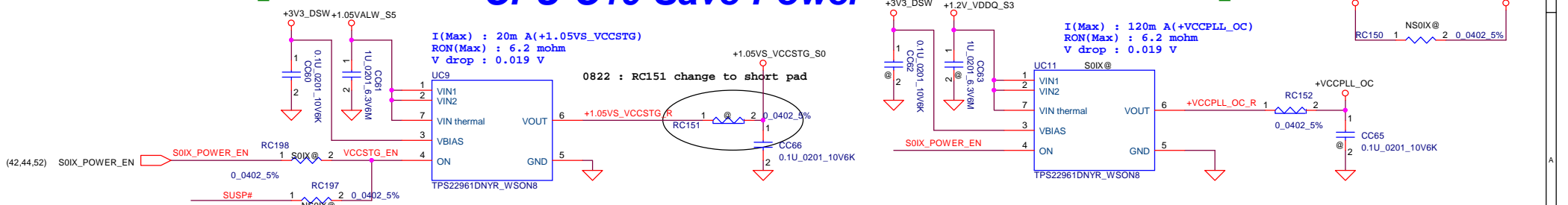
change package of 1U from 0201 to 0402



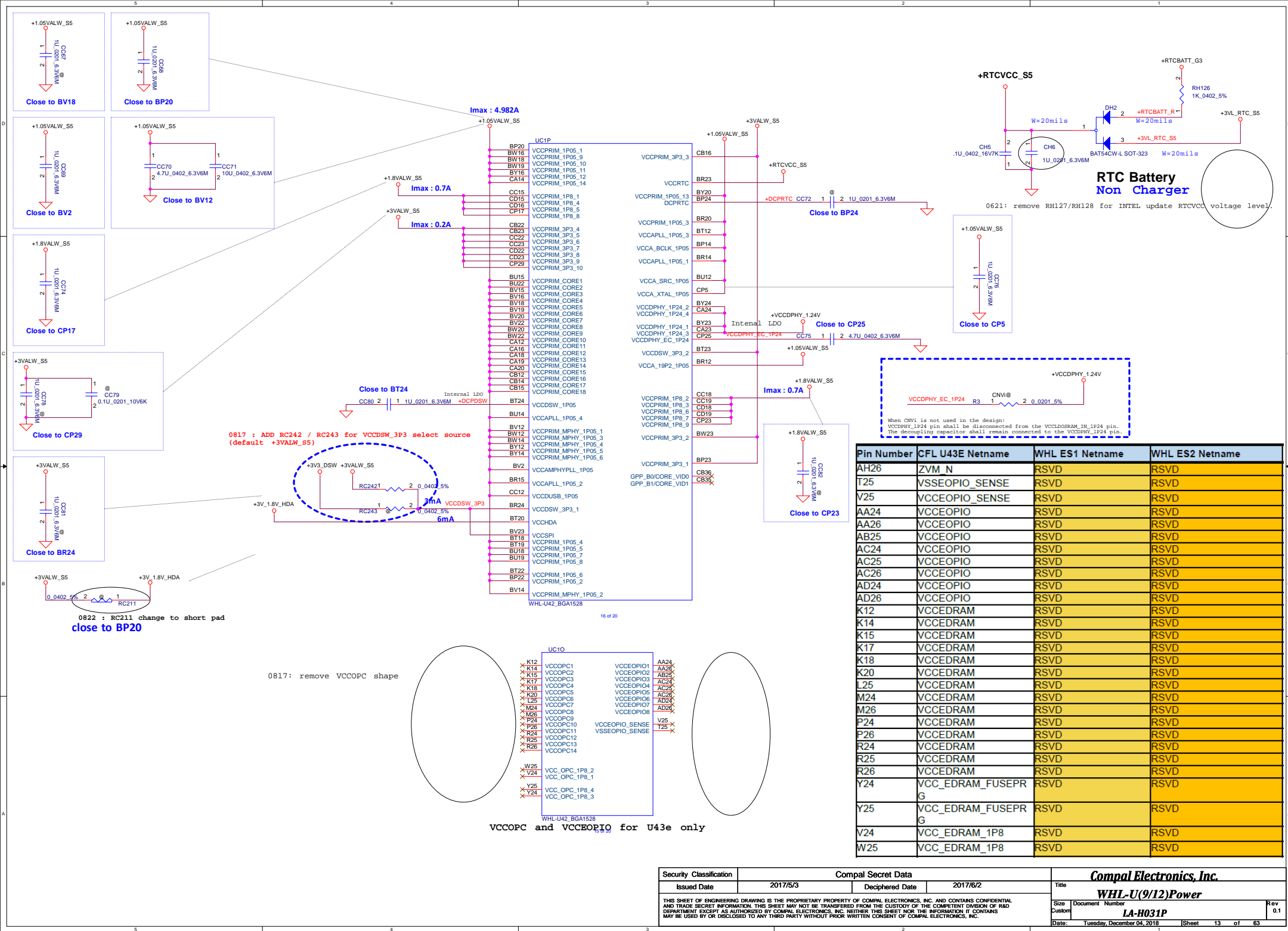
+1.05VALW TO +1.05VS_VCCSTG

CPU C10 Save Power

+1.2V TO +VCCPLL_OC



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/5/3	Deciphered Date	2017/6/2	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				WHL-U(8/12)Power	
Size	Document Number	Rev		LA-H031P	
Custom				0.1	
Date:		Tuesday, December 04, 2018		Sheet	12 of 63



Pin Number	CFL U43E Netname	WHL ES1 Netname	WHL ES2 Netname
AH26	ZVM_N	RSVD	RSVD
T25	VSSEOPIO_SENSE	RSVD	RSVD
V25	VCCEOPIO_SENSE	RSVD	RSVD
AA24	VCCEOPIO	RSVD	RSVD
AA26	VCCEOPIO	RSVD	RSVD
AB25	VCCEOPIO	RSVD	RSVD
AC24	VCCEOPIO	RSVD	RSVD
AC25	VCCEOPIO	RSVD	RSVD
AC26	VCCEOPIO	RSVD	RSVD
AD24	VCCEOPIO	RSVD	RSVD
AD26	VCCEOPIO	RSVD	RSVD
K12	VCCEDRAM	RSVD	RSVD
K14	VCCEDRAM	RSVD	RSVD
K15	VCCEDRAM	RSVD	RSVD
K17	VCCEDRAM	RSVD	RSVD
K18	VCCEDRAM	RSVD	RSVD
K20	VCCEDRAM	RSVD	RSVD
L25	VCCEDRAM	RSVD	RSVD
M24	VCCEDRAM	RSVD	RSVD
M26	VCCEDRAM	RSVD	RSVD
P24	VCCEDRAM	RSVD	RSVD
P26	VCCEDRAM	RSVD	RSVD
R24	VCCEDRAM	RSVD	RSVD
R25	VCCEDRAM	RSVD	RSVD
R26	VCCEDRAM	RSVD	RSVD
Y24	VCC_EDRAM_FUSEPRG	RSVD	RSVD
Y25	VCC_EDRAM_FUSEPRG	RSVD	RSVD
V24	VCC_EDRAM_1P8	RSVD	RSVD
W25	VCC_EDRAM_1P8	RSVD	RSVD

+VCC_CORE_S0

+VCC_CORE_S0

+VCC_GT_S0

+VCC_GT_S0

0928:
+VCCGT_VCCCORE_S0
rename to +VCC_CORE_S0

+VCC_CORE_S0

Trace Length Match < 25 mils

+1.05V_VCCSTG_S0

SVID ALERT

Place the PU
resistors close to CPU

Place the PU
resistors close to CPU

UC1M

A5 VCCGT8 VCCGT58 D15
A6 VCCGT9 VCCGT59 D17
A8 VCCGT10 VCCGT60 D18
A12 VCCGT11 VCCGT61 D20
A14 VCCGT12 VCCGT64 F5
A15 VCCGT13 VCCGT69 F6
A17 VCCGT14 VCCGT70 F7
A18 VCCGT15 VCCGT71 F8
A20 VCCGT16 VCCGT72 F11
A21 VCCGT17 VCCGT73 F14
A22 VCCGT18 VCCGT74 F17
A23 VCCGT19 VCCGT75 F20
A24 VCCGT20 VCCGT76 G11
A25 VCCGT21 VCCGT77 G12
A26 VCCGT22 VCCGT78 G14
A27 VCCGT23 VCCGT79 G15
A28 VCCGT24 VCCGT80 G17
A29 VCCGT25 VCCGT81 G20
A30 VCCGT26 VCCGT82 H5
A31 VCCGT27 VCCGT83 H6
A32 VCCGT28 VCCGT84 H7
A33 VCCGT29 VCCGT85 H8
A34 VCCGT30 VCCGT86 H11
A35 VCCGT31 VCCGT87 H12
A36 VCCGT32 VCCGT88 H14
A37 VCCGT33 VCCGT89 H15
A38 VCCGT34 VCCGT90 H17
A39 VCCGT35 VCCGT91 H18
A40 VCCGT36 VCCGT92 H20
A41 VCCGT37 VCCGT93 J7
A42 VCCGT38 VCCGT94 J8
A43 VCCGT39 VCCGT95 J11
A44 VCCGT40 VCCGT96 J14
A45 VCCGT41 VCCGT97 J17
A46 VCCGT42 VCCGT98 J20
A47 VCCGT43 VCCGT99 K2
A48 VCCGT44 VCCGT100 K11
A49 VCCGT45 VCCGT101 L7
A50 VCCGT46 VCCGT102 L8
A51 VCCGT47 VCCGT103 L10
A52 VCCGT48 VCCGT104 M9
A53 VCCGT49 VCCGT105 N7
A54 VCCGT50 VCCGT106 N8
A55 VCCGT51 VCCGT107 N9
A56 VCCGT52 VCCGT108 N10
A57 VCCGT53 VCCGT109 P2
A58 VCCGT54 VCCGT110 P8
A59 VCCGT55 VCCGT111 R9
A60 VCCGT56 VCCGT112 T8
A61 VCCGT57 VCCGT113 T9
A62 VCCGT58 VCCGT114 T10
A63 VCCGT59 VCCGT115 U8
A64 VCCGT60 VCCGT116 U10
A65 VCCGT61 VCCGT117 V2
A66 VCCGT62 VCCGT118 V8
A67 VCCGT63 VCCGT119 W8
A68 VCCGT64 VCCGT120 W9
A69 VCCGT65 VCCGT121 Y8
A70 VCCGT66 VCCGT122 Y9

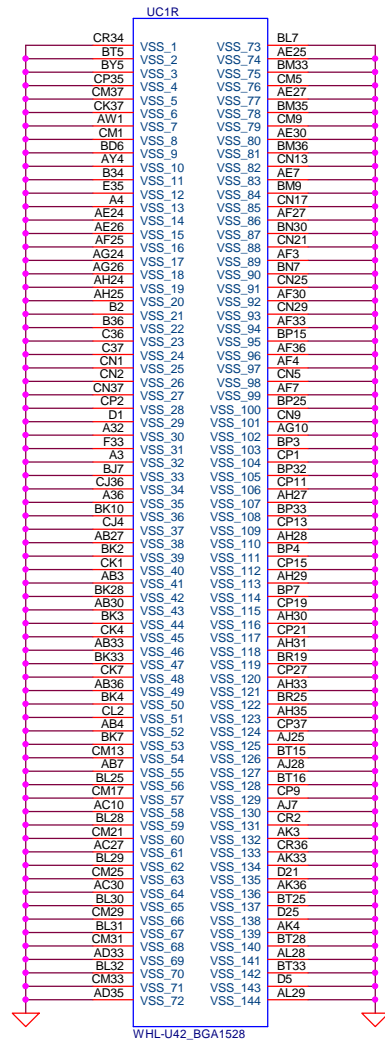
WHL-U42_BGA1528

13 of 20

VCCGT_SENSE
VSSGT_SENSE

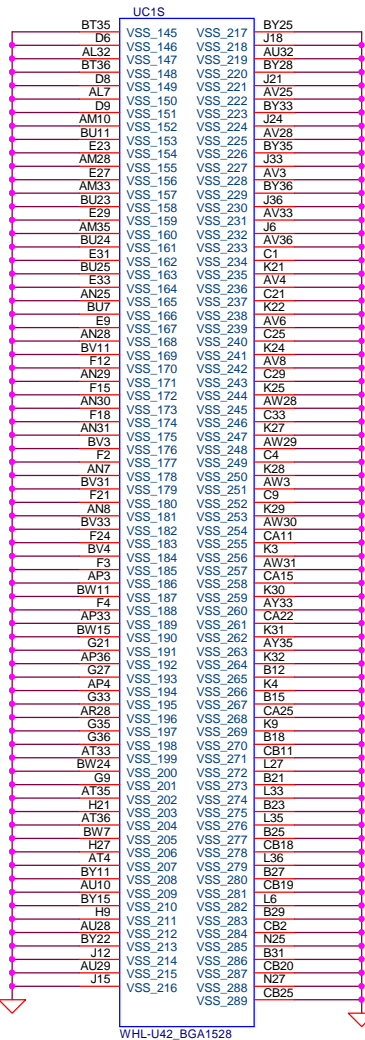
Trace Length Match < 25 mils

Pin Number	CFL-U43E	WHL ES1 Netname	WHL ES2 Netname
AA9	VCCGT	VCCGT	VCCCORE
AB10	VCCGT	VCCGT	VCCCORE
AB2	VCCGT	VCCGT	VCCCORE
AB8	VCCGT	VCCGT	VCCCORE
AB9	VCCGT	VCCGT	VCCCORE
AC8	VCCGT	VCCGT	VCCCORE
AD9	VCCGT	VCCGT	VCCCORE
AE10	VCCGT	VCCGT	VCCCORE
AE8	VCCGT	VCCGT	VCCCORE
AE9	VCCGT	VCCGT	VCCCORE
AF10	VCCGT	VCCGT	VCCCORE
AF2	VCCGT	VCCGT	VCCCORE
AF8	VCCGT	VCCGT	VCCCORE
AG8	VCCGT	VCCGT	VCCCORE
AG9	VCCGT	VCCGT	VCCCORE
AH9	VCCGT	VCCGT	VCCCORE
AJ10	VCCGT	VCCGT	VCCCORE
AJ8	VCCGT	VCCGT	VCCCORE
AK2	VCCGT	VCCGT	VCCCORE
AK9	VCCGT	VCCGT	VCCCORE
AL10	VCCGT	VCCGT	VCCCORE
AL8	VCCGT	VCCGT	VCCCORE
AL9	VCCGT	VCCGT	VCCCORE
AM8	VCCGT	VCCGT	VCCCORE
V2	VCCGT	VCCGT	VCCCORE
Y10	VCCGT	VCCGT	VCCCORE
Y8	VCCGT	VCCGT	VCCCORE



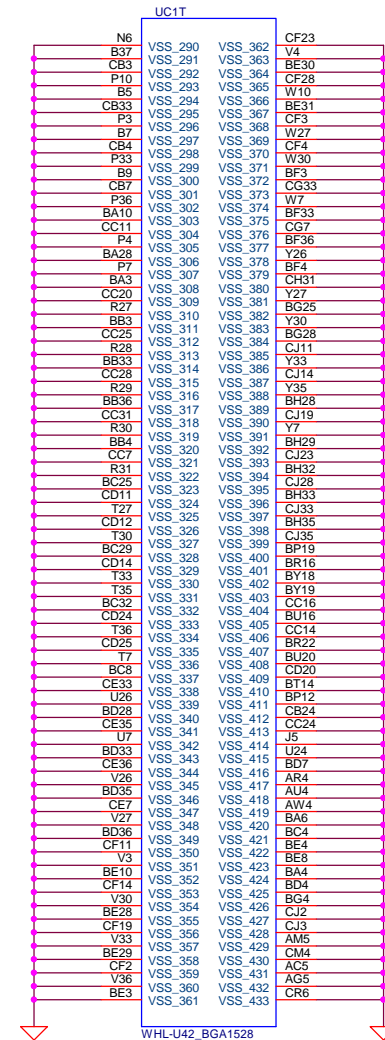
WHL-U42_BGA1528

17 of 20



WHL-U42_BGA1528

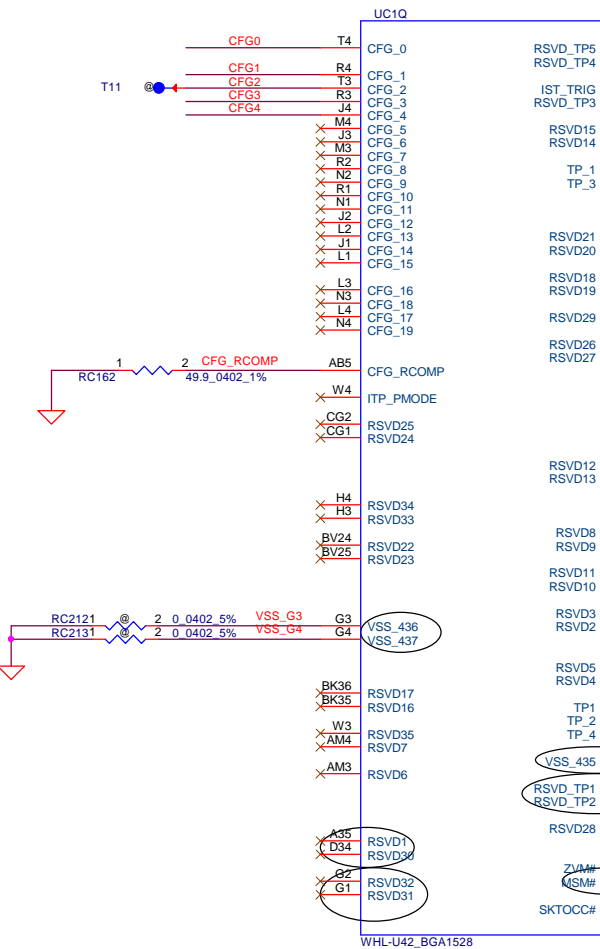
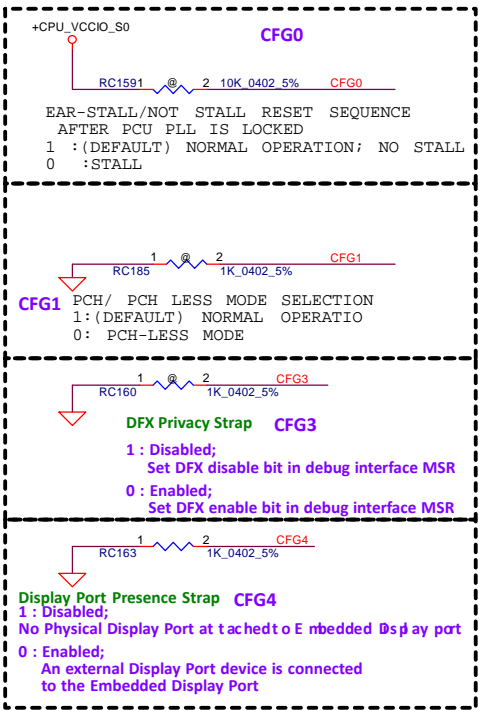
18 of 20



WHL-U42_BGA1528

19 of 20

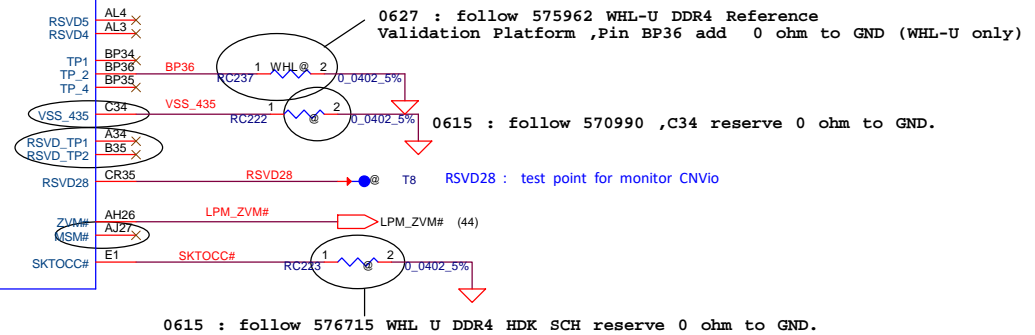
Security Classification		Compal Secret Data		Title	
Issued Date	2017/5/3	Deciphered Date	2017/6/2	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				WHL-U(11/12)GND	
Size	Document Number	Rev		0.1	
Custom	LA-H031P				
Date:	Tuesday, December 04, 2018	Sheet	15	of	63



Pin Number	CFL U43E Netname	WHL ES1 Netname	WHL ES2 Netname
AJ27	MSM_N	RSVD	RSVD
B35	EDRAM_VIEW[1]	RSVD	RSVD
A34	EDRAM_VIEW[0]	RSVD	RSVD
G4	EDRAM_THERMDC	RSVD	RSVD
G3	EDRAM_THERMDA	RSVD	RSVD
L5	EDRAM_OPIO_RCOMP	RSVD	RSVD
C34	EDRAM_EDM	RSVD	RSVD
G1	EANALOGVP[1]	RSVD	RSVD
G2	EANALOGVP[0]	RSVD	RSVD
D34	CPU_EOPIO_VIEW[1]	RSVD	RSVD
A35	CPU_EOPIO_VIEW[0]	RSVD	RSVD
N5	CPU_EOPIO_RCOMP	RSVD	RSVD

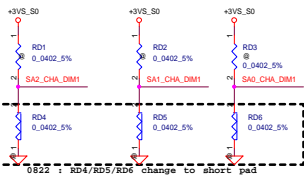
RSVD

All the RSVD pins should be left unconnected (floating) on the board.
575412_WHL-U Schematic Checklist



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/5/3	Deciphered Date	2017/6/2	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	LA-H031P
				Date:	Tuesday, December 04, 2018
				Sheet	16 of 63
				Rev	0.1

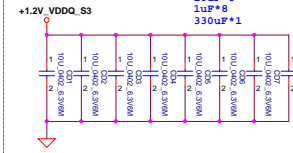
INTERLEAVE



PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

STRETCH GOAL IS 2133 M175

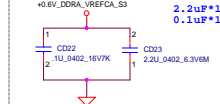
Layout Note:
Place near JDIMM1



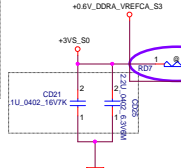
(4.0 mm) REV TYPE



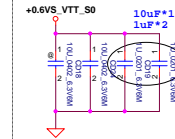
Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM1



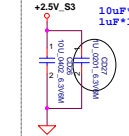
PLACE NEAR TO PIN



Layout Note:
Place near JDIMM1



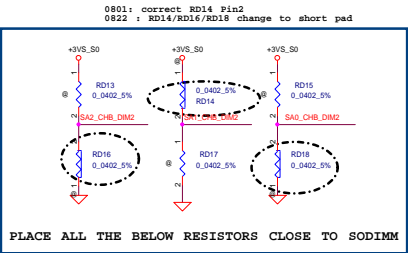
Layout Note:
Place near JDIMM



www.teknisi-indonesia.com

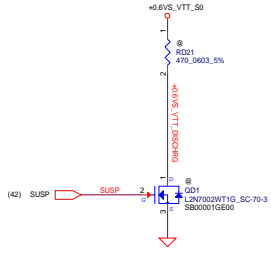
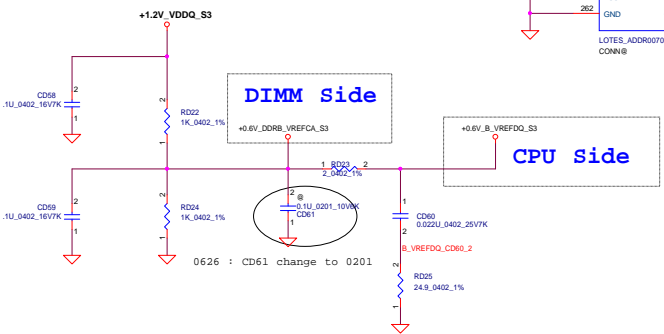
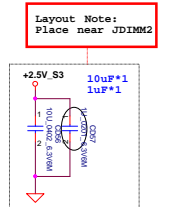
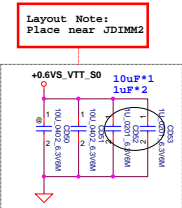
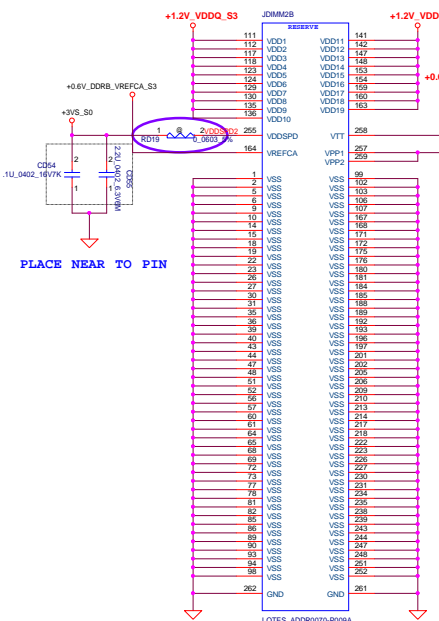
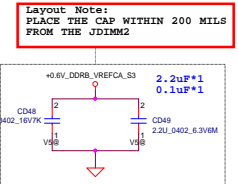
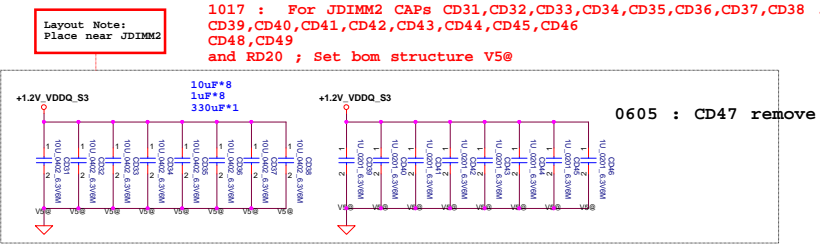
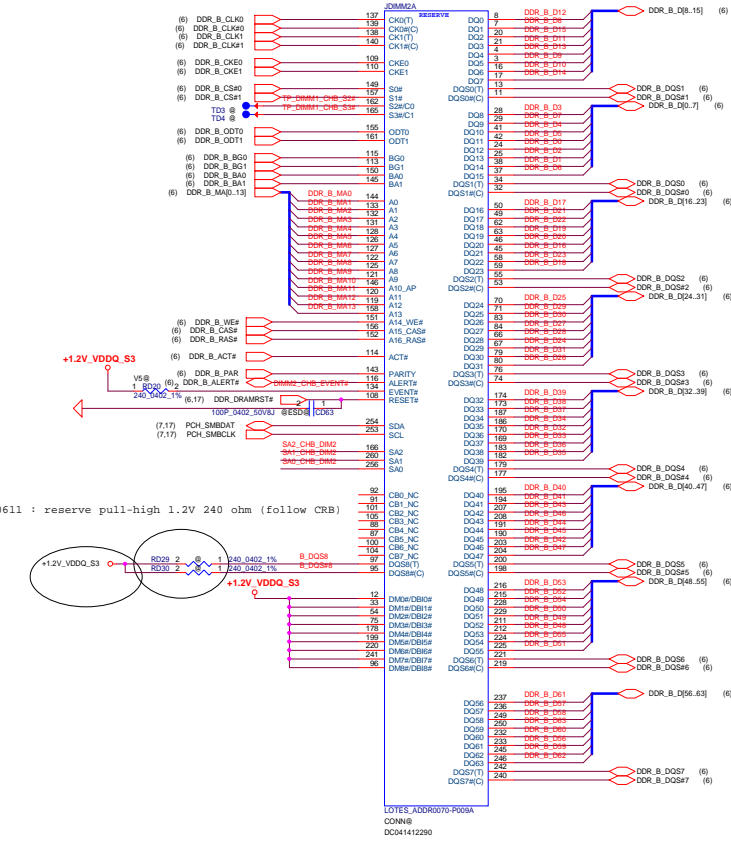
Security Classification	Compul Secret Data		Compul Electronics, Inc.	
Issued Date	2015/12/25	Deciphered Date	2015/12/31	Title
THIS SHEET OF ENGINEERING DRAWINGS IS THE PROPRIETARY PROPERTY OF COMPAUL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D OR REPRODUCED OR BE AUTHORIZED BY COMPAUL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION THEREON MAY BE USED OR COPIED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAUL ELECTRONICS, INC.			Size	Document Number
			Custm	LA-H031P
			Date	Tuesday, December 29, 2015 17 of 23

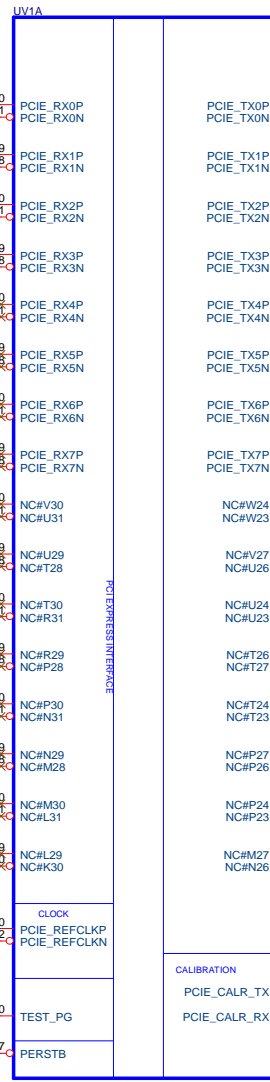
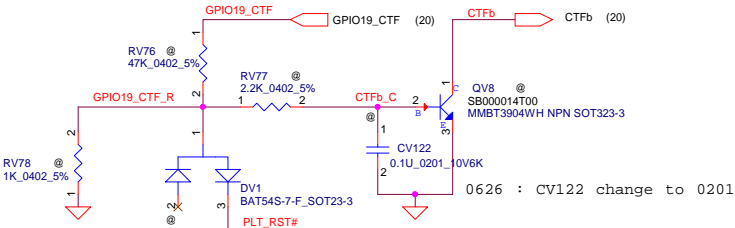
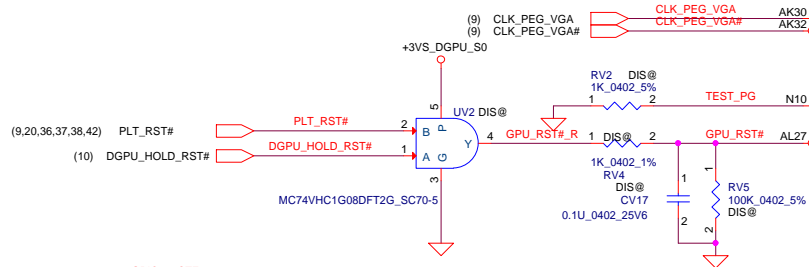
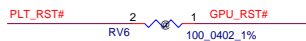
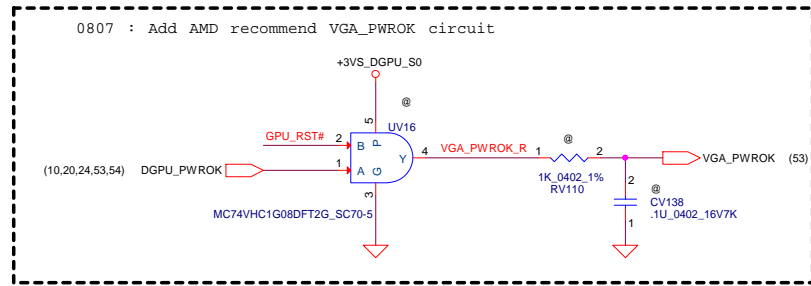
INTERLEAVE CHANNEL-B



SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0xa4
READ ADDRESS: 0xa5
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

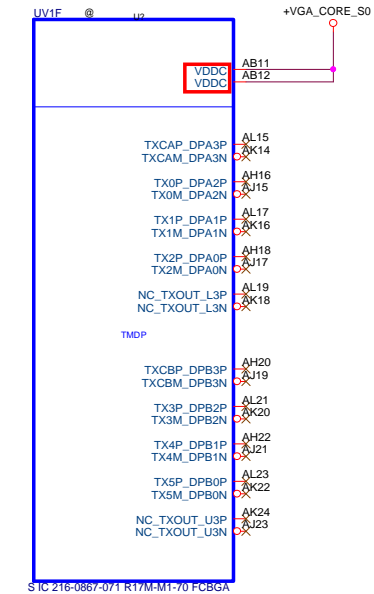
(8.0 mm) REV TYPE





SA000098VF0

No Use GPU Display Port output



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/10/01	Deciphered Date	2016/10/01	Title	R17M-M1-70(1/5) PCIE
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Custom
				Document Number	LA-H031P
				Rev	1A
				Date:	Tuesday, December 04, 2018
				Sheet	19 of 63

Reserve VROM

+3VS_DGPU_S0

RV84 10K_0402_5%

CV123 0.1U_0402_25V6

GPIO6 1 2 RV85 33_0402_5%

GPIO9 1 2 RV86 33_0402_5%

GPIO10 1 2 RV87 33_0402_5%

GPIO22 1 2 RV89 33_0402_5%

ROM_SO

S1A16

SCKWEB

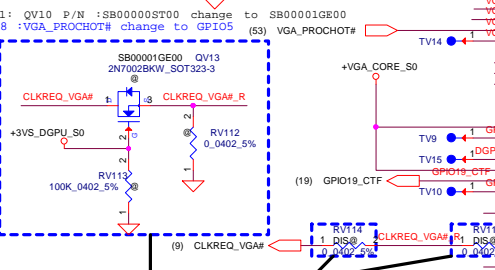
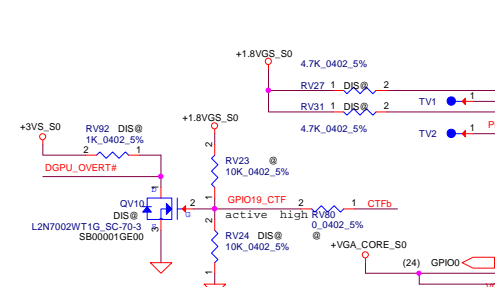
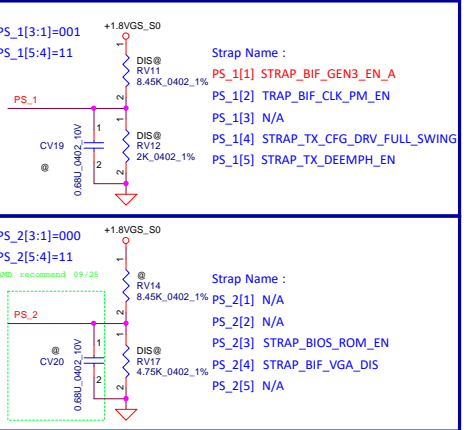
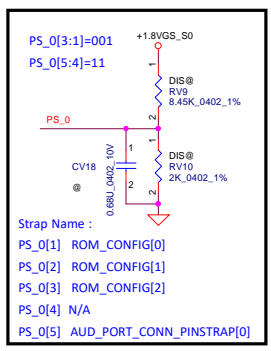
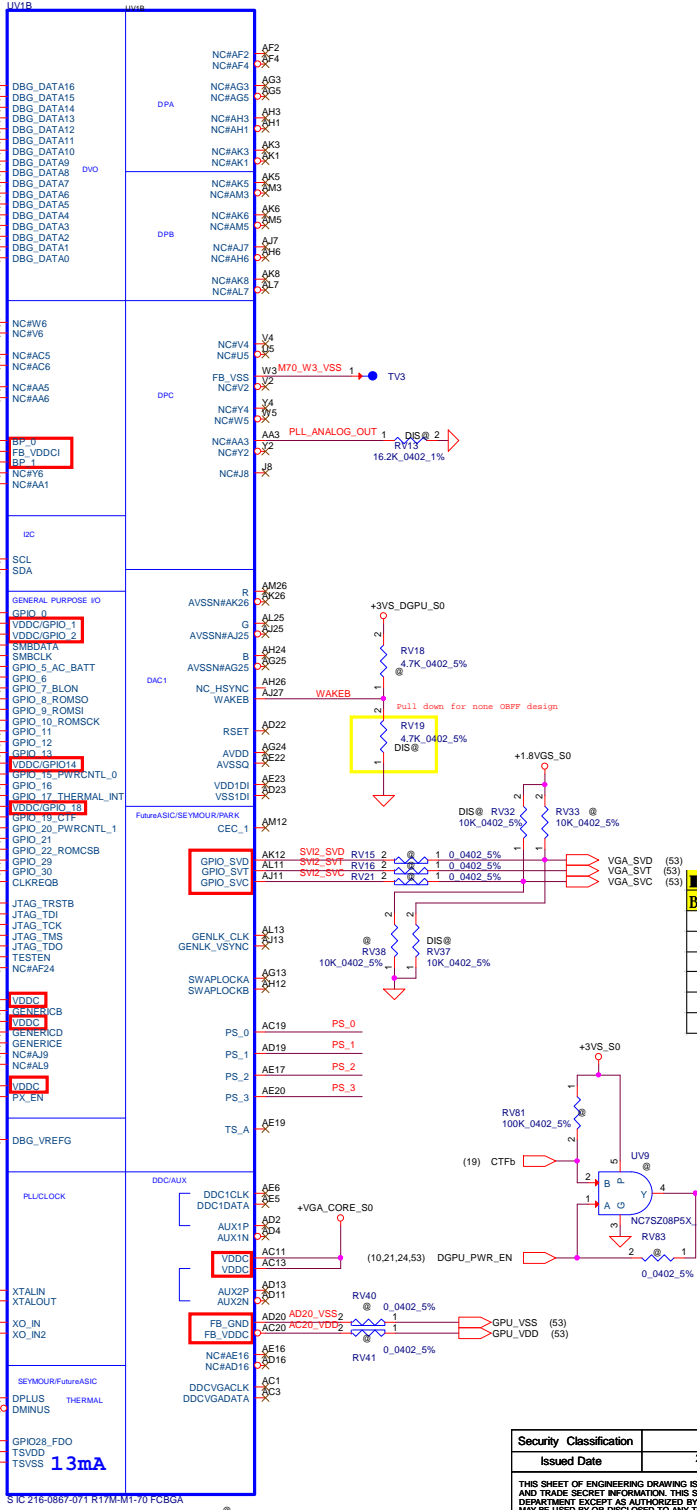
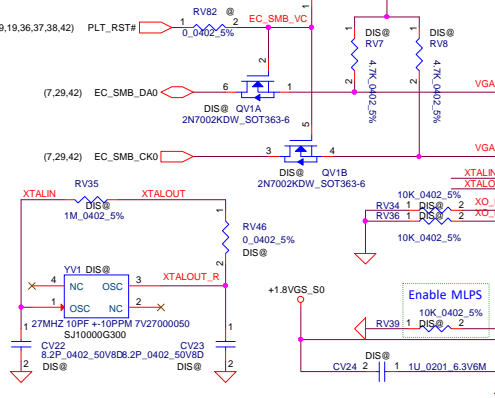
UV8_W#

HOLD

VCC

VSS

M25P10-AVMM6T_S08

[illegible]

PS_0[3] romidfg_2	PS_0[2] romidfg_1	PS_0[1] romidfg_0	Memory Aperture Size
0	0	0	128 MB
0	0	1	256 MB
0	1	0	64 MB
0	1	1	Reserved
1	0	0	512 MB-Not Supported
1	0	1	1 GB-Not Supported
1	1	0	2 GB-Not Supported
1	1	1	4 GB-Not Supported

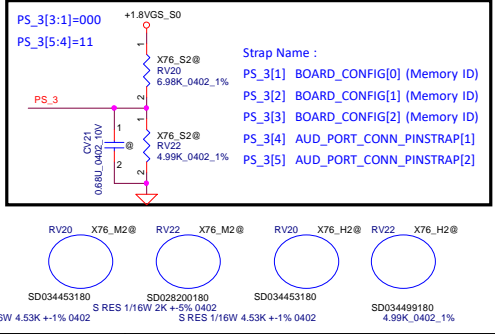
Frame Buffer Size	Memory Aperture Size
64 MB	64 MB
128 MB	128 MB
256 MB	256 MB
512 MB or Larger	256 MB

Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

R _{pu} (ohm)	R _{pd} (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

SLPS MEMORY ID Setting:						
Board Config[2:0]		Memory Type	Configuration	Channel Size	Vendor P/N	Compal P/N
ID	[2:0]					
0	000	Samsung gDDR5	128Mx32 2PCS	1GB	K4G41325F6-HC28	SA00009IT40
1	001	Hynix gDDR5	128Mx32 2PCS	1GB	H56C4H24AJR-T2C	SA00009HQ00
2	010	Micron gDDR5	256Mx32 2PCS	2GB NEW	MT5J256M32HF-70-B	SA00009IV60
3	011	Samsung gDDR5	256Mx32 2PCS	2GB	K4G80325F6-HC28	SA00009ZD10
4	100	Hynix gDDR5	256Mx32 2PCS	2GB NEW	H5GCBH24AJR-ROC	SA00009UI50

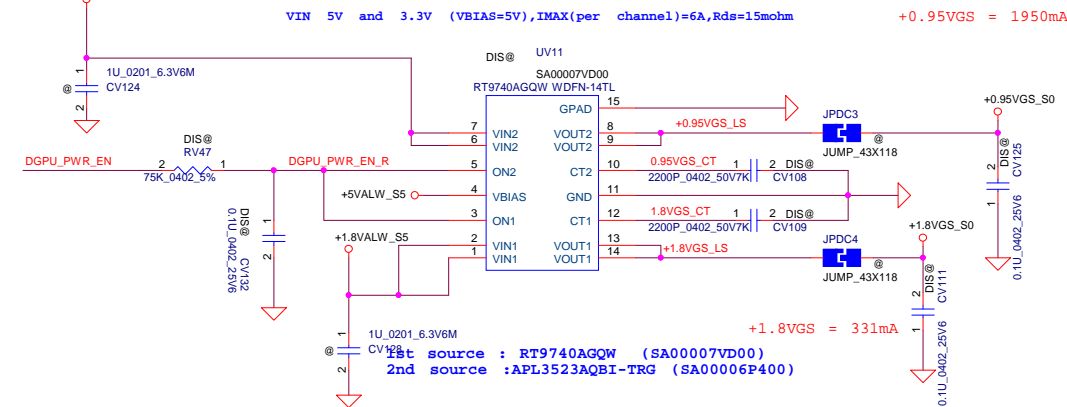
X7676338L01	:	RV20	=	6.98K	,	RV22	=	4.99K	(SAMSUNG 2G)
X7676338L02	:	RV20	=	4.53K	,	RV22	=	4.99K	(MICRON 2G)
X7676338L03	:	RV20	=	4.53K	,	RV22	=	2K	(HYNIX 2G)



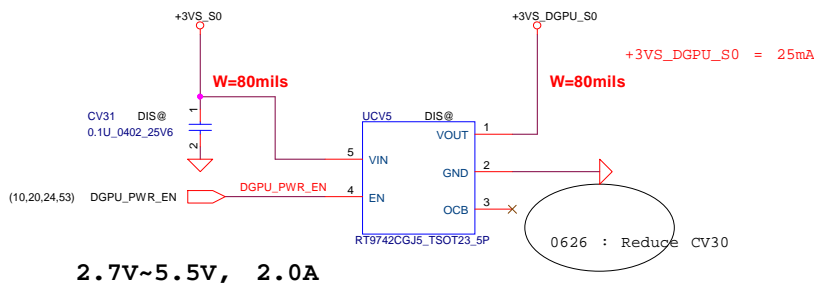
Security Classification		Compal Secret Data		Compal Electronics, Inc.					
Issued Date		2015/10/01	Deciphered Date		2016/10/01	Title			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						R17M-M1-70(2/5)_MSIC			
						Size	Document Number		Rev
						Cust	LA-H031P		1A
						Date:	Tuesday, December 04, 2018	Sheet	20
4				5					

**+1.8VGS
+0.95VGS
Load switch**

+CPU_VCCIO_S0

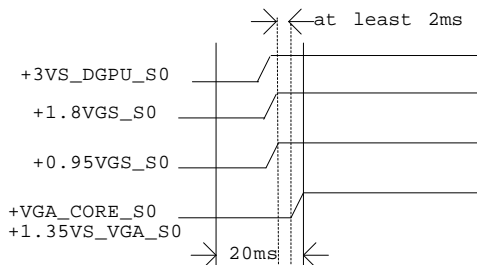


+3VS to +3VGS

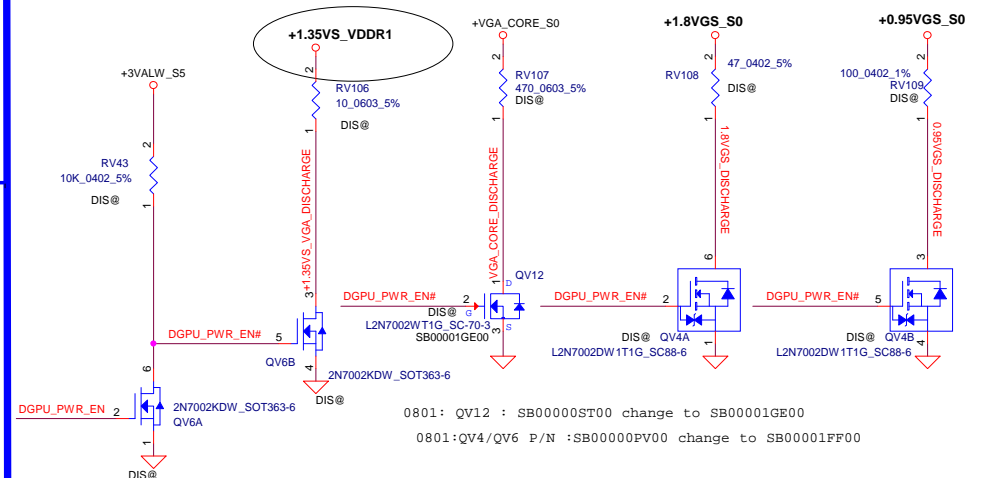
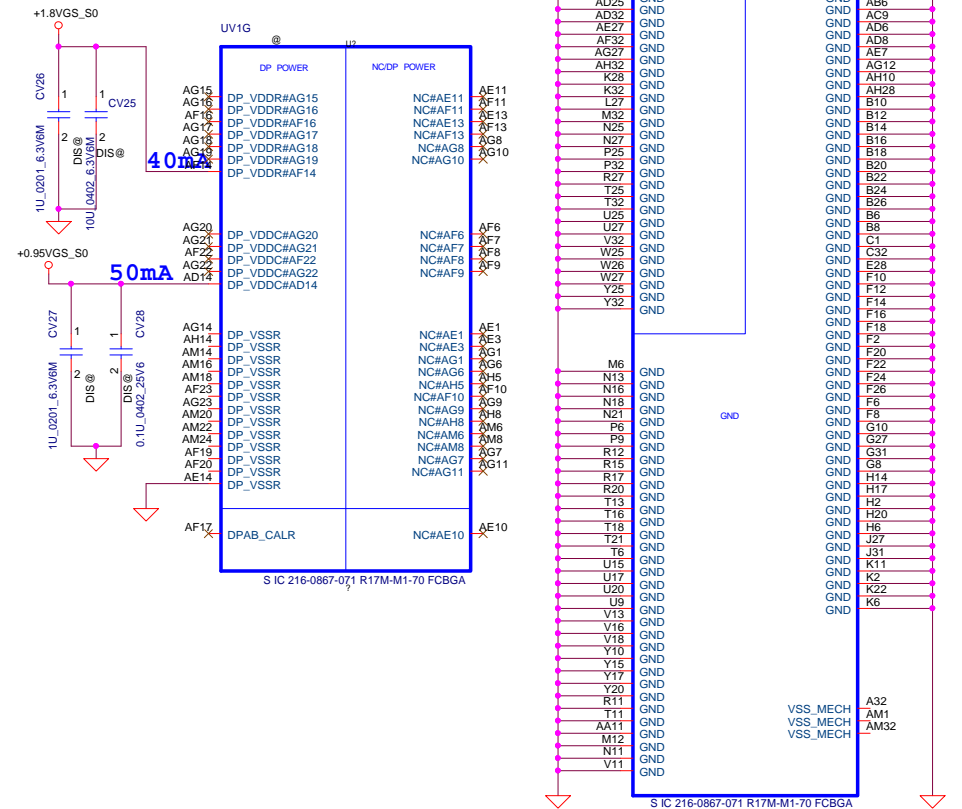


All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ μ s.

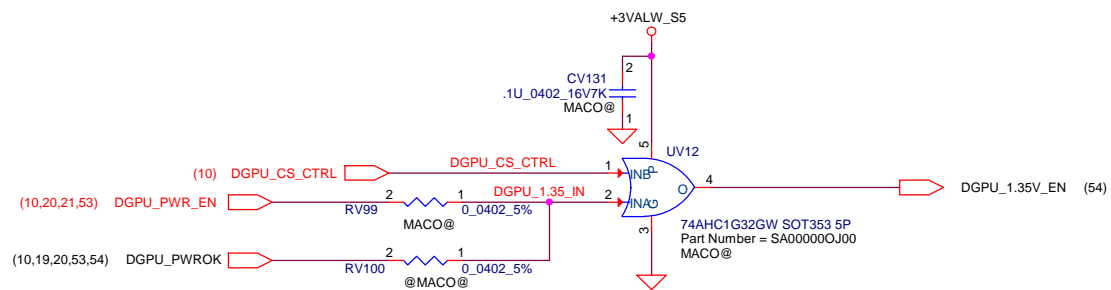
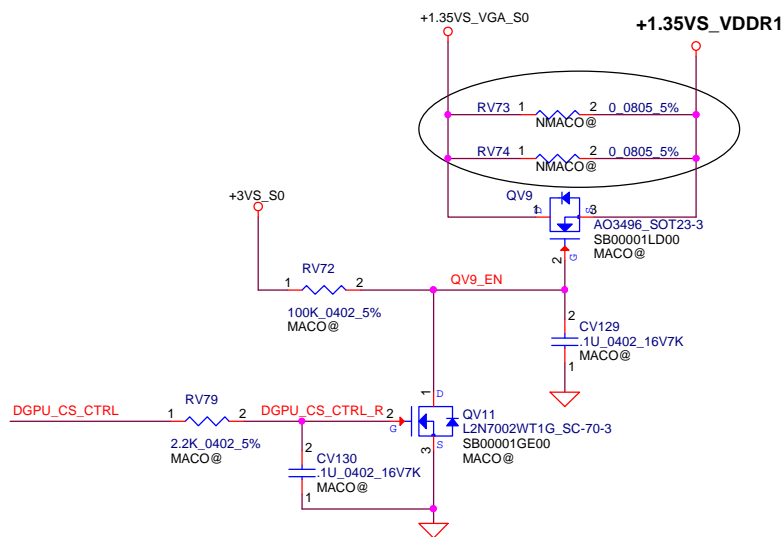
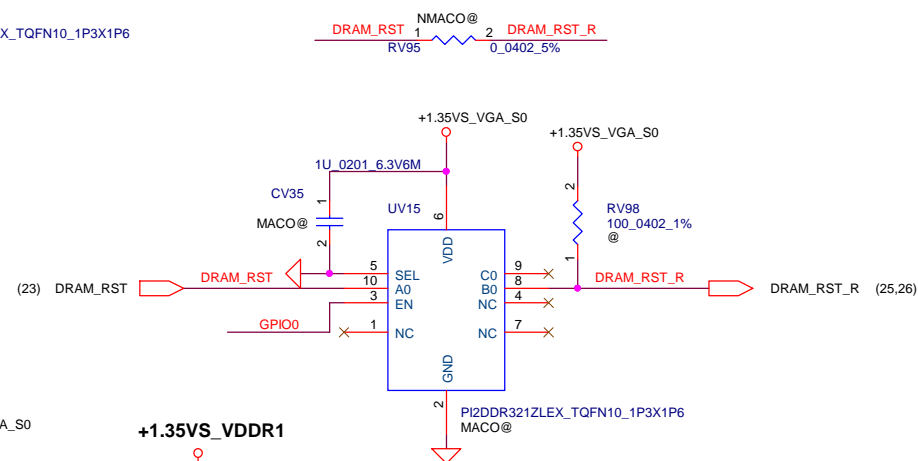
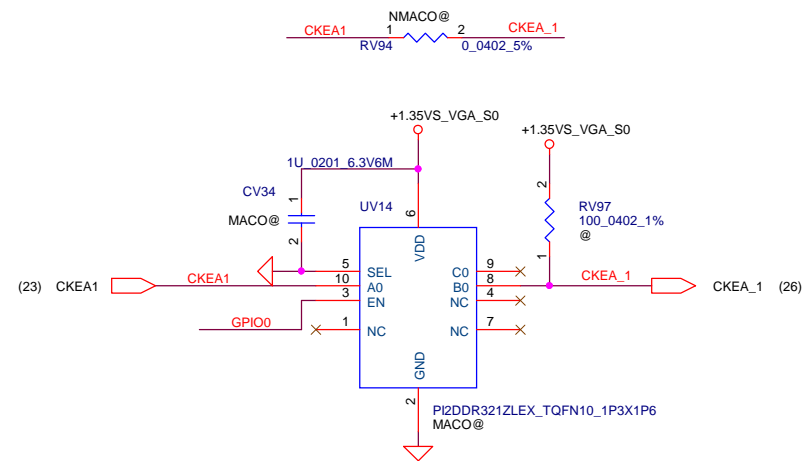
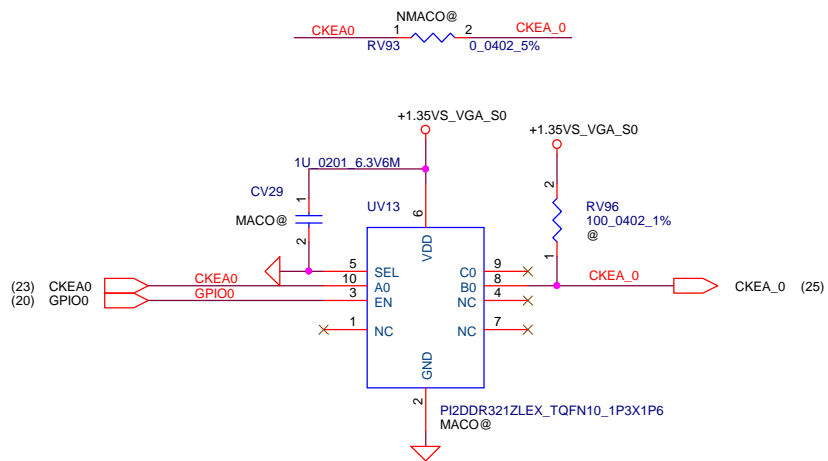
- 1.the 3.3-V rail ramp up first.
- 2.the 0.95-V rail reach at least 90% of its nominal value no later than 2 ms from the start of VDDC ramping up



No Use GPU Display Port output

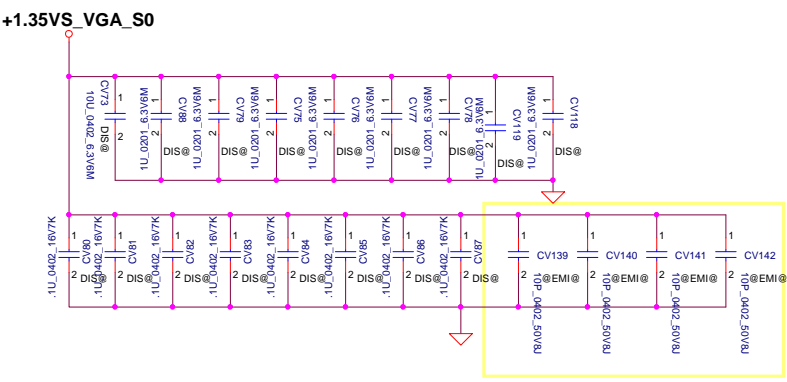
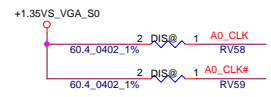
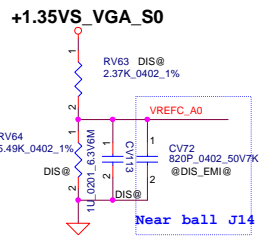
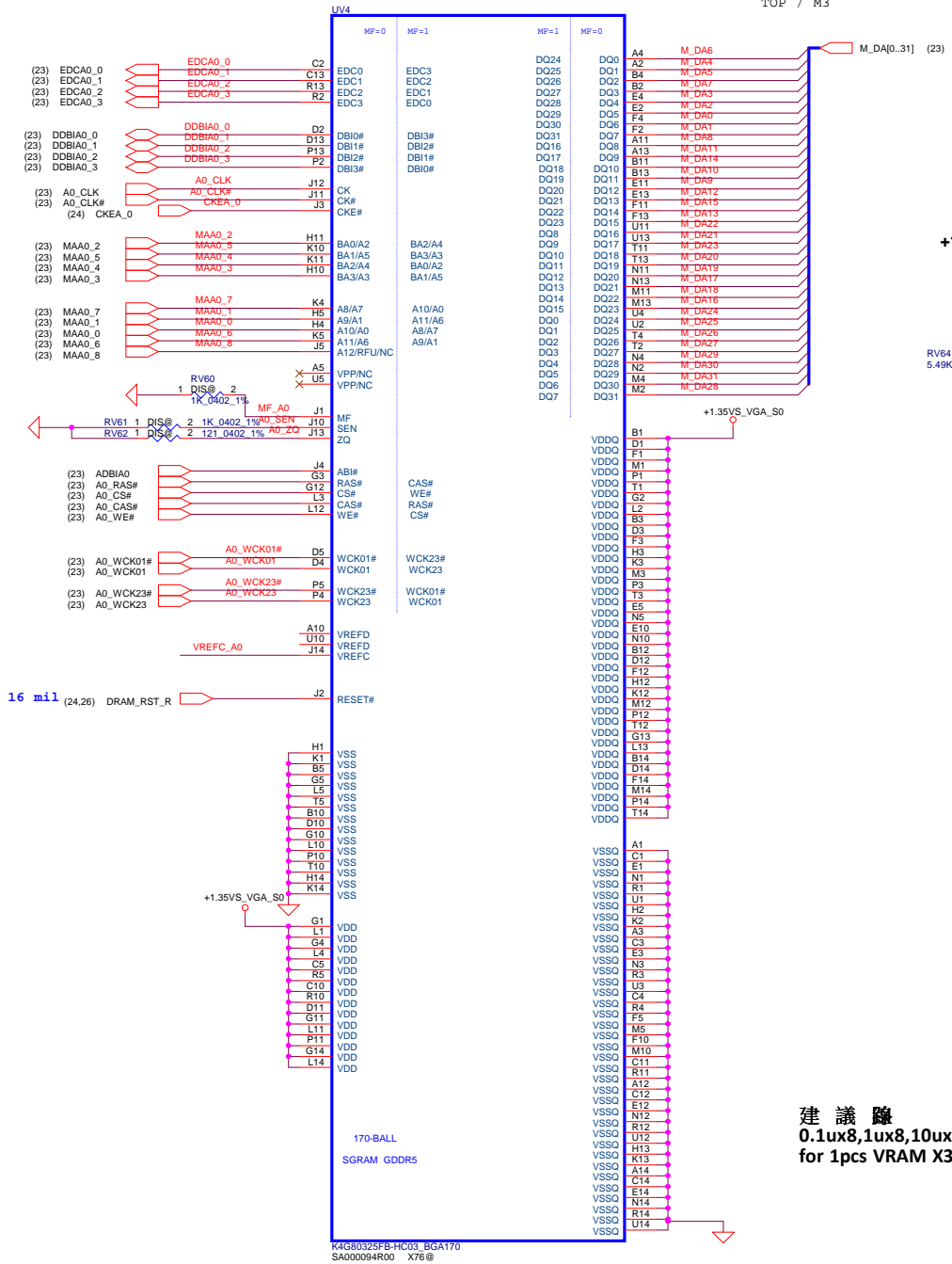


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/10/01	Deciphered Date	2016/10/01	Title	R17M-M1-70 (3/5)_PWR/GND
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Custom
				Document Number	LA-H031P
				Rev	1A
				Date:	Tuesday, December 04, 2018
				Sheet	21 of 63



Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2015/10/01		Deciphered Date		2016/10/01		Title			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						R17M-M1-70(6/6)_VDDR1					
						Size		Document Number		Rev	
						Custom		LA-F901P M/B		0.1	
						Date: Tuesday, December 04, 2018				Sheet 24 of 63	

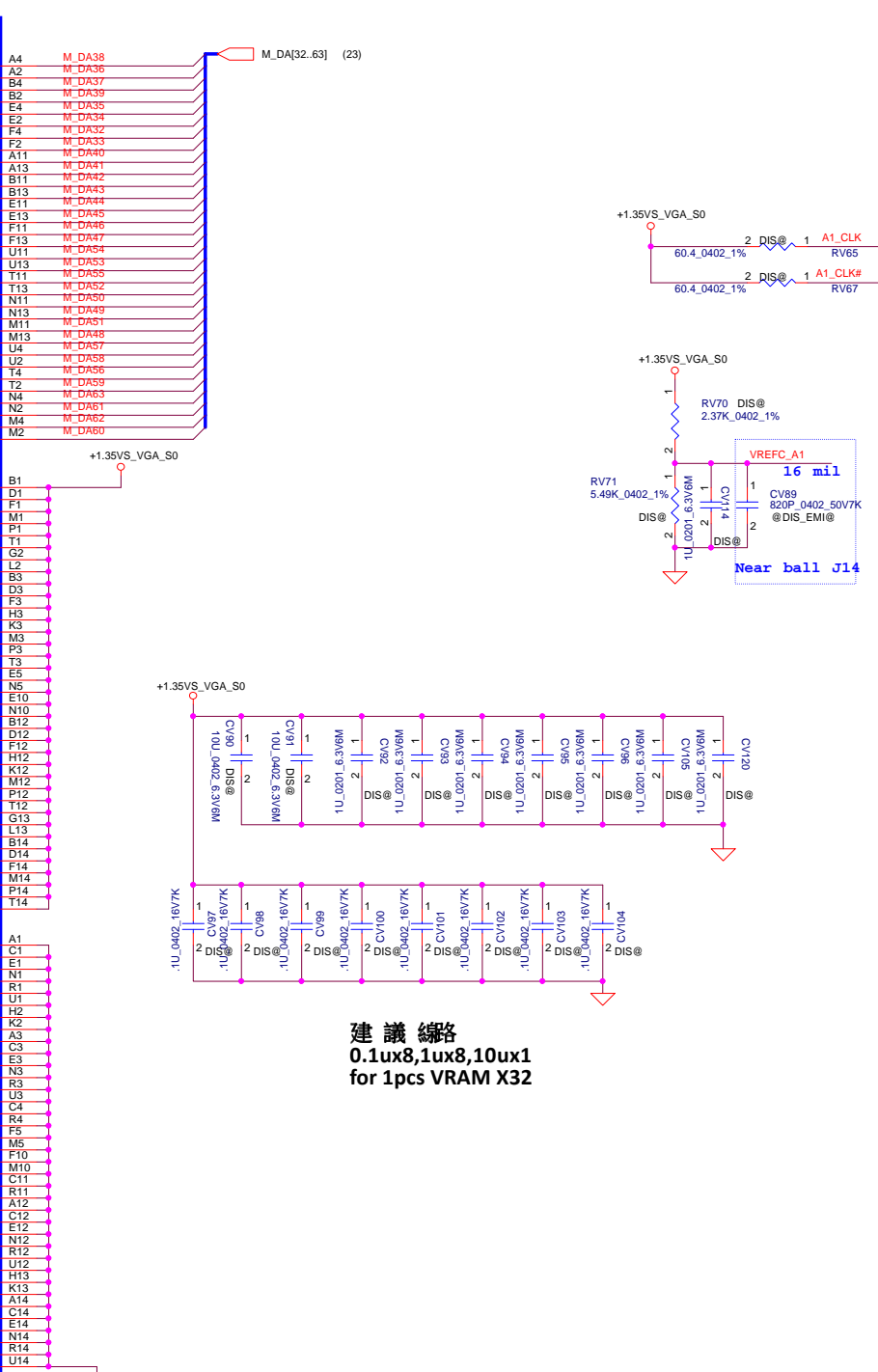
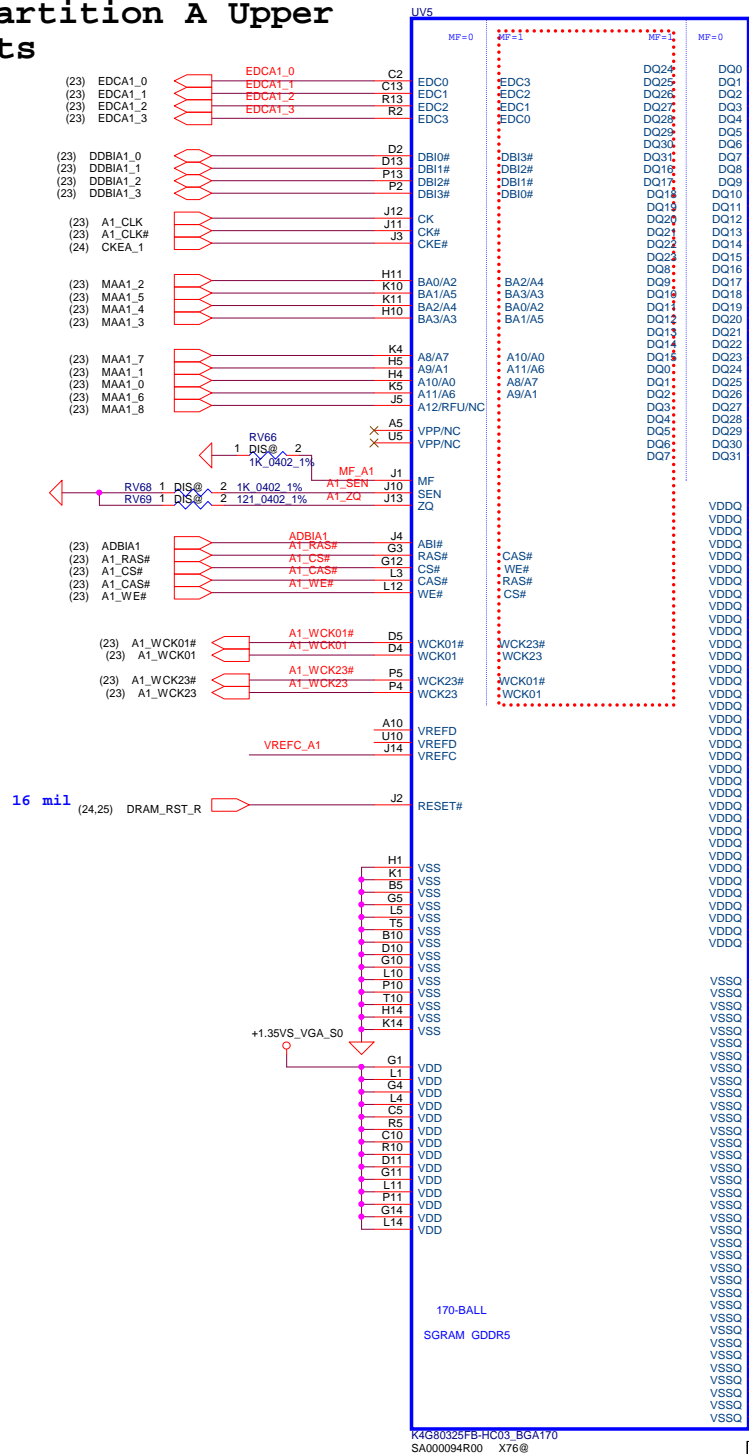
Memory Partition A Lower
-32 bits



建議
0.1ux8,1ux8,10ux1
for 1pcs VRAM X32

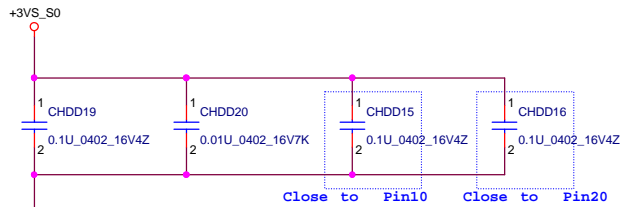
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/03/01	Deciphered Date	2014/03/01	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RAD DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				GDDR5 VRAM A Lower	
Size		Document Number		Rev	
		LA-F901P M/B		0.1	
Date:		Tuesday, December 04, 2018		Sheet 25 of 63	

5	
Memory Partition A Upper	
- 32 bits	

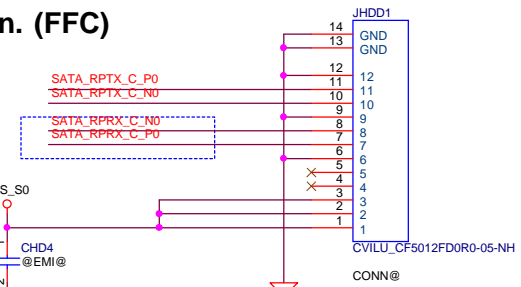


Security Classification		Compal Secret Data		Compal Electronics, Inc.					
Issued Date		2013/03/01	Deciphered Date	2014/03/01	Title				
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					GDDR5 A Upper				
					Size		Document	Number	Rev
								LA-F901P M/B	0.1
					Date:		Tuesday, December 04, 2018	Sheet	26

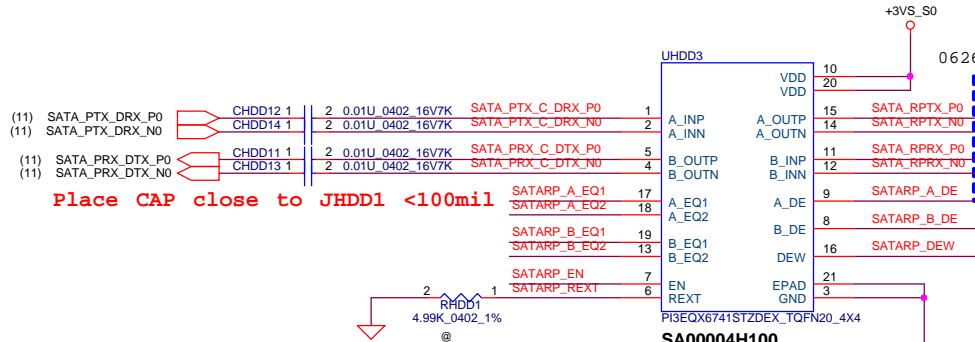
SATA HDD Conn. (FFC)



0704: JHDD1 Pin8 Pin7 Swap



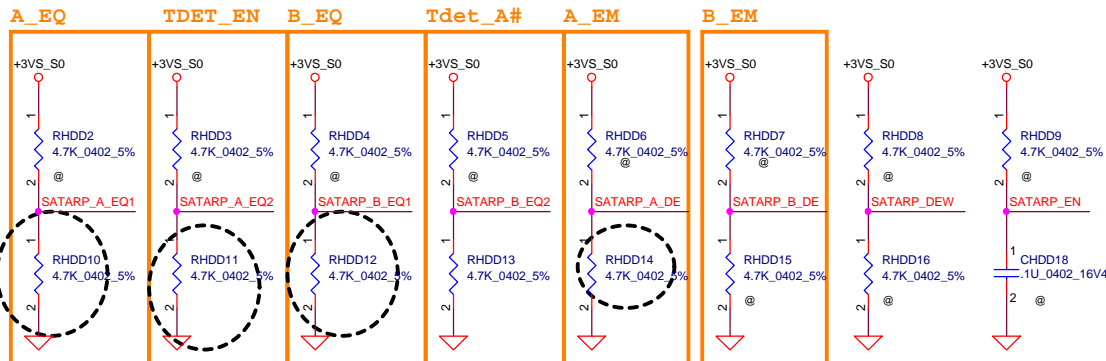
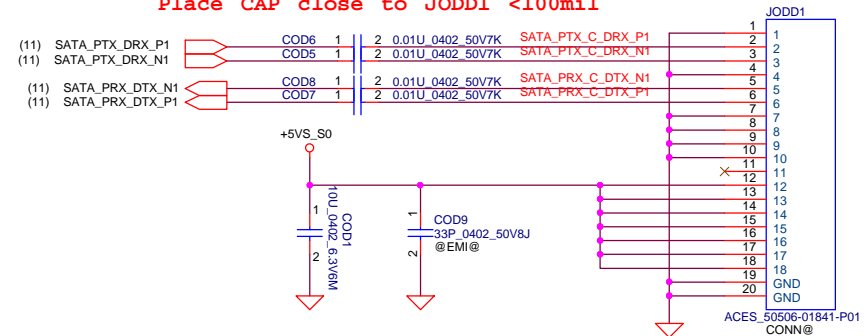
1008: For DFB request change footprint to cvilu_cf5012fd0r0-05-nh_l2p-s



0626 : HDD Redriver change to PI3EQX6741STZDEX
0628 : FAE suggest default adjustment setting Pin let it floating.

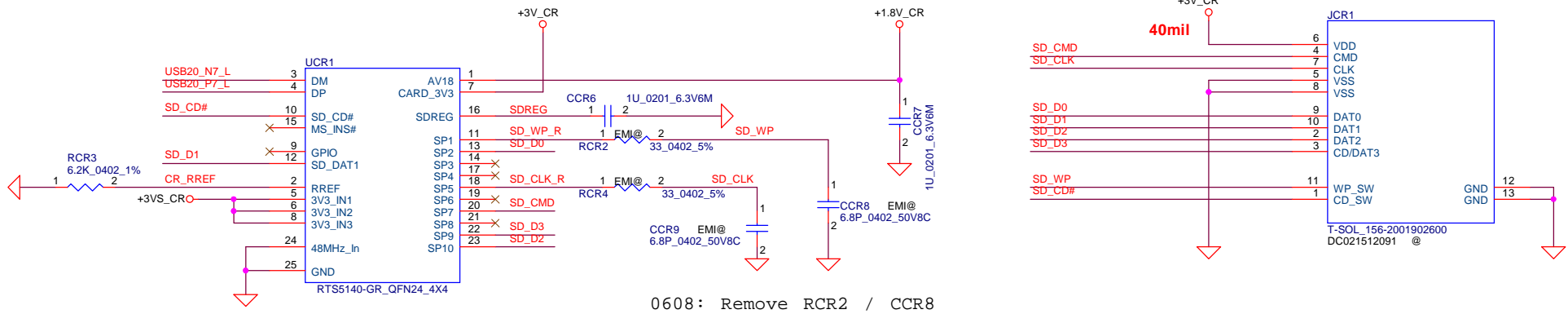
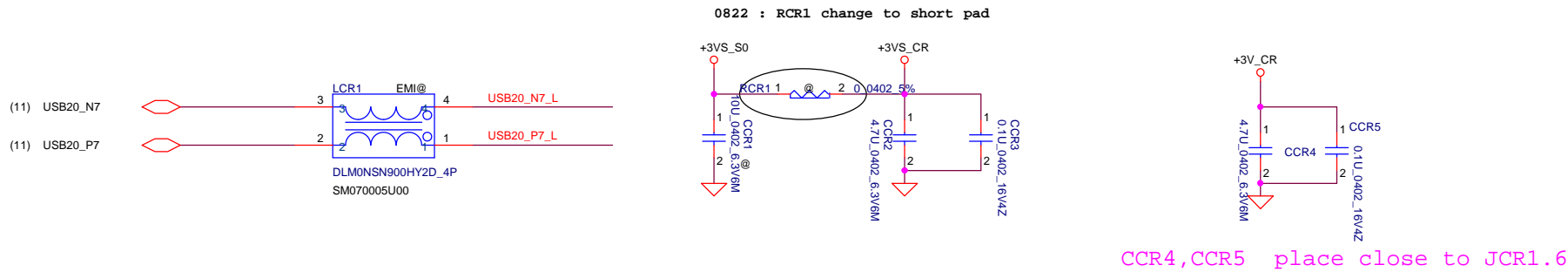
SATA ODD Conn. (FFC)

Place CAP close to JODD1 <100mil



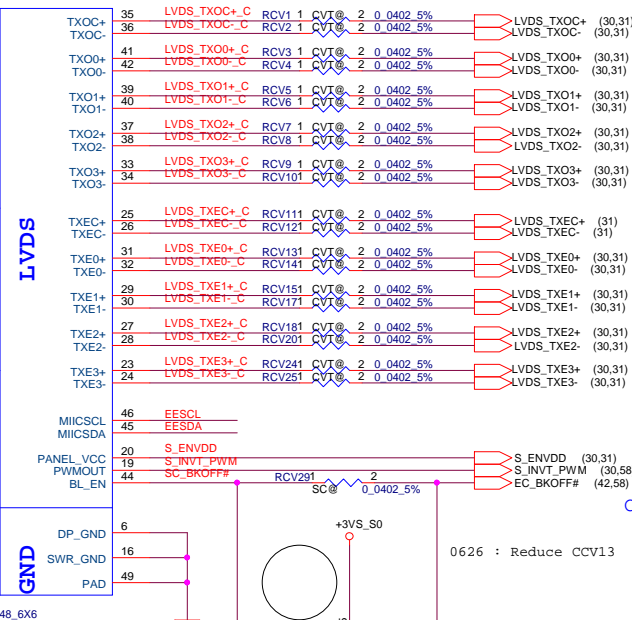
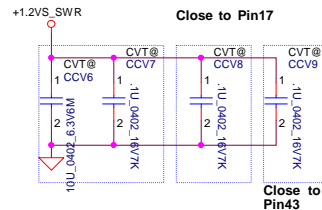
0817 : reference FAE test result
The setting was changed like below:
Pin9: A_EM=low, RHDD14=4.7kohm
Pin17: A_EQ=Low, RHDD10=4.7kohm
Pin18: TDET_EN=low, RHDD11=4.7kohm
Pin19: B_EQ=Low, RHDD12=4.7kohm

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/12/25	Deciphered Date	2013/09/01	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				HDD+redriver/ODD	
Size	Document	Number	Rev	Date: Tuesday, December 04, 2018	
Custom			0.1	Sheet 27 of 63	

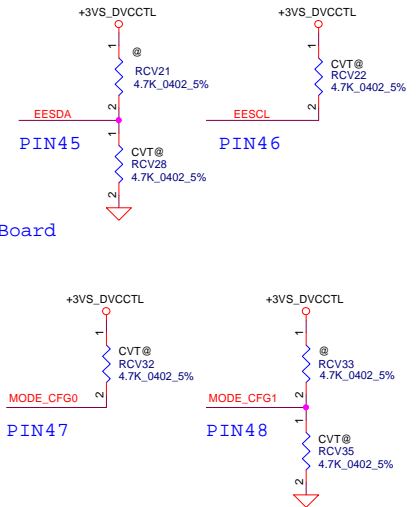


0608: Remove RCR2 / CCR8

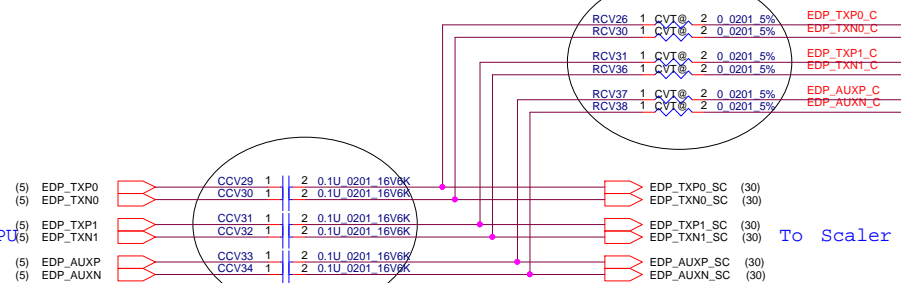
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/12/25	Deciphered Date	2013/09/01	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				CardReader RTS5140	
				Size Custom	Document Number LA-H031P
				Date:	Rev
				Tuesday, December 04, 2018	1.0
				Sheet	28 of 63



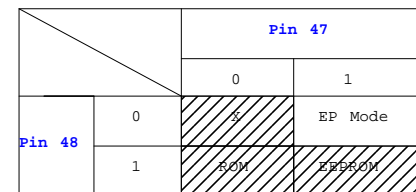
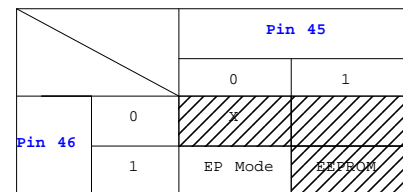
LVDS CONNECTOR

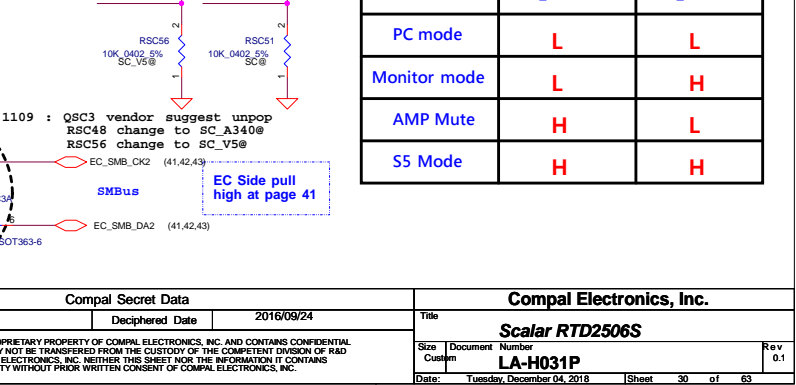
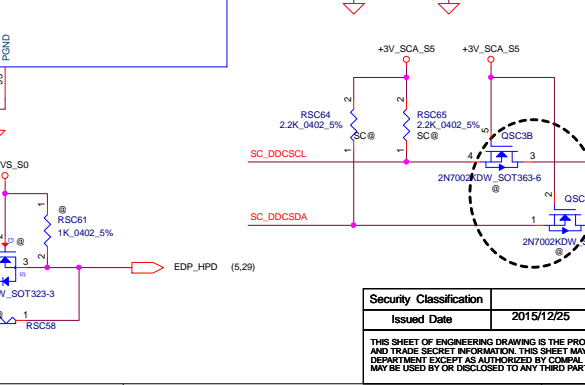
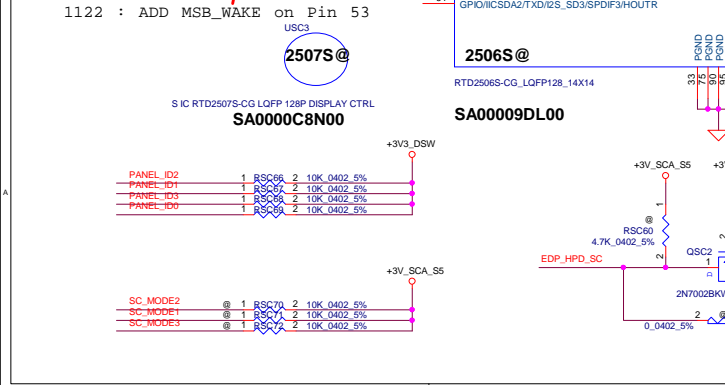


Converter Board



To LVDS Convertor IC





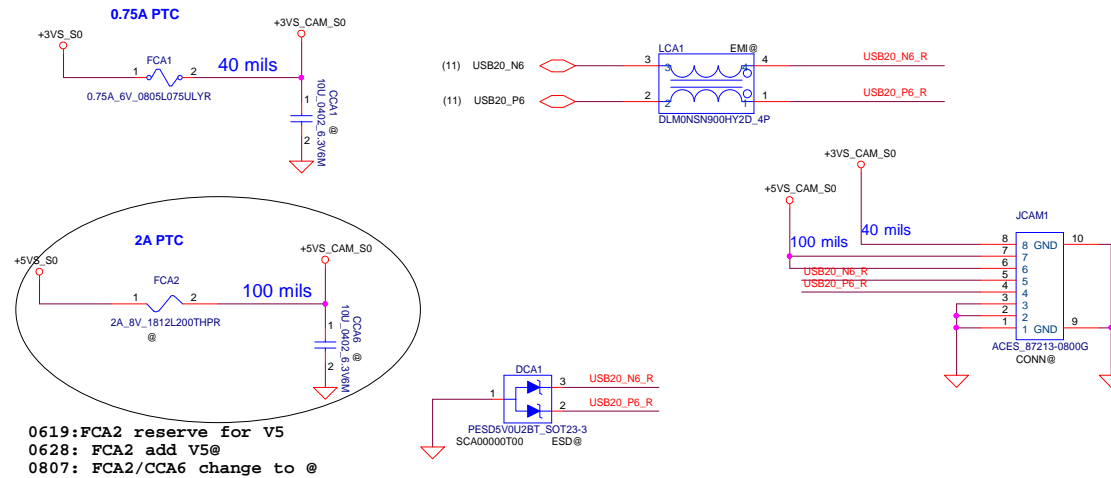
SC_SMLCLK 2 1 RSC53 PM_SMBCLK (7,41)
0_0402_5%

SC_SMLDAT 2 1 RSC54 PM_SMBDAT (7,41)
0_0402_5%

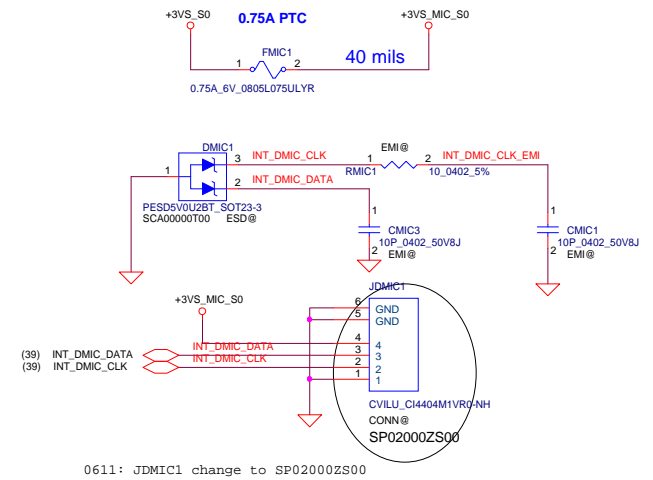
	SC_MODE1	SC_MODE2
PC mode	L	L
Monitor mode	L	H
AMP Mute	H	L
S5 Mode	H	H

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2015/12/25	Deciphered Date	2016/09/24	Title	Scalar RTD2506S	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				Customer	LA-H031P	0.1
				Date:	Tuesday, December 04, 2018	Sheet 30 of 63

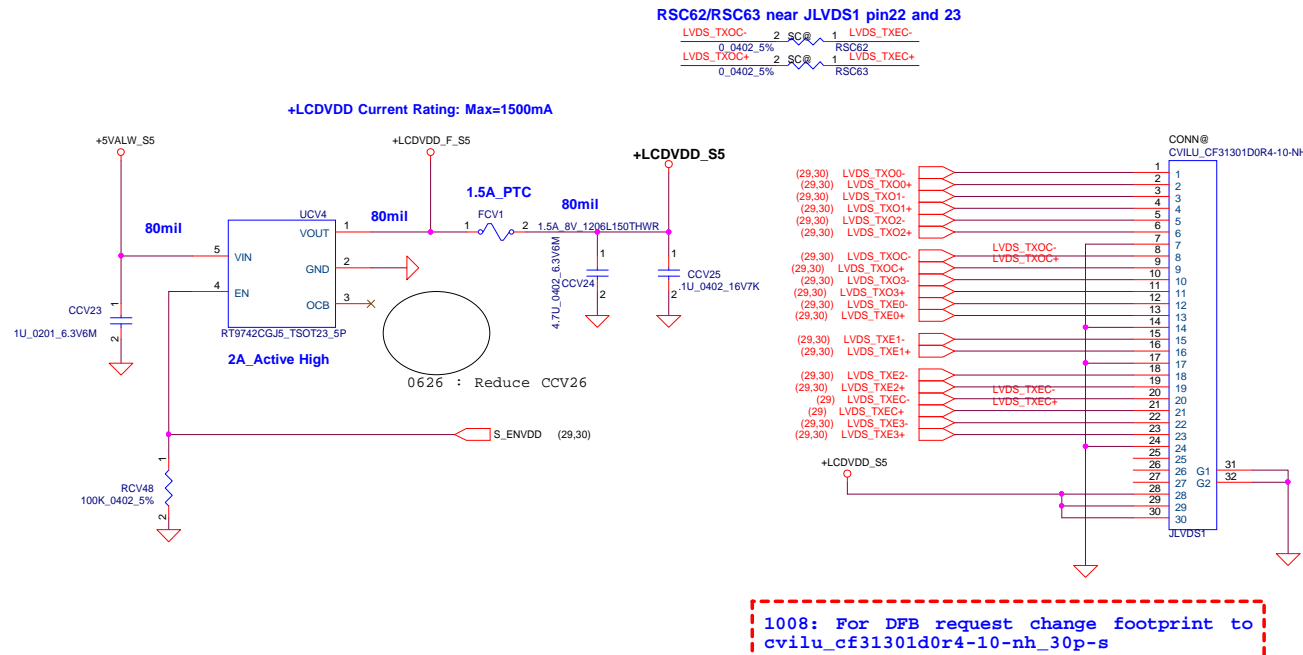
CAMERA



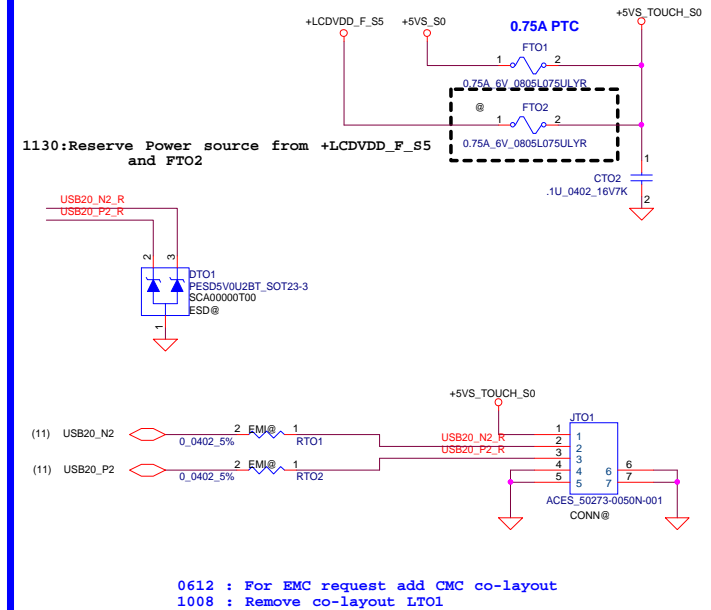
DMIC



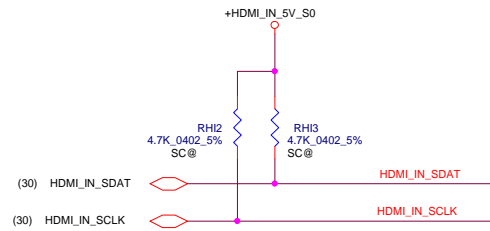
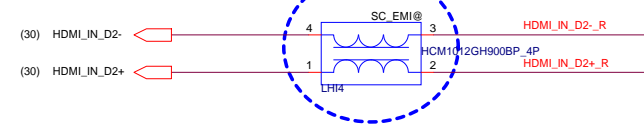
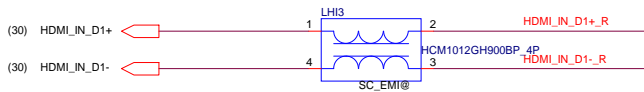
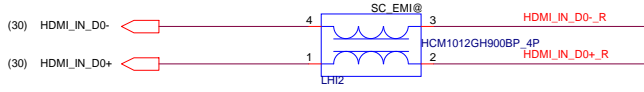
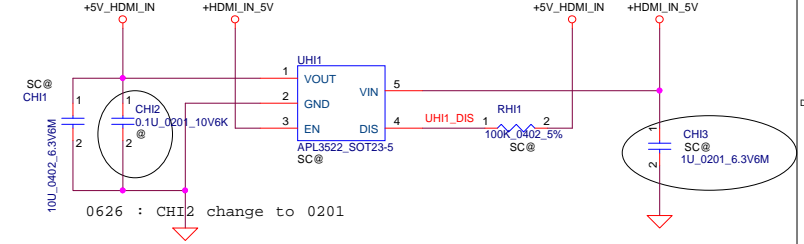
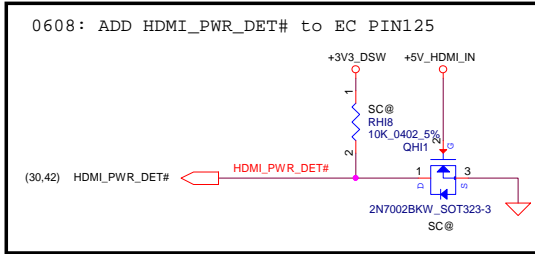
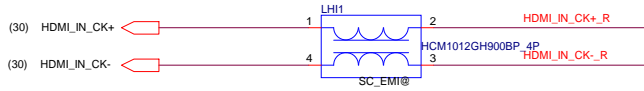
LVDS



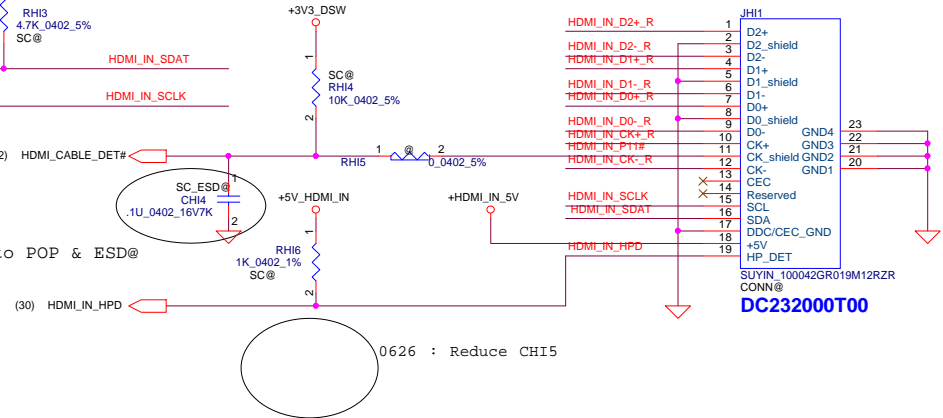
Touch



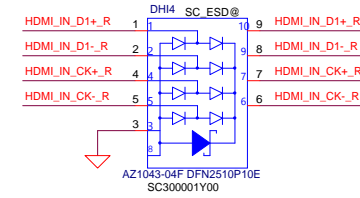
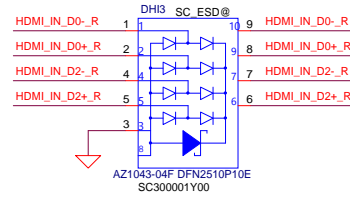
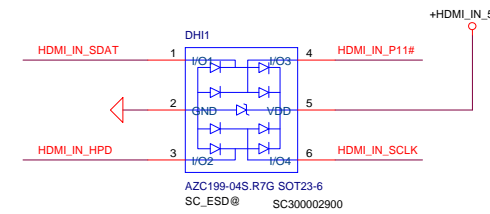
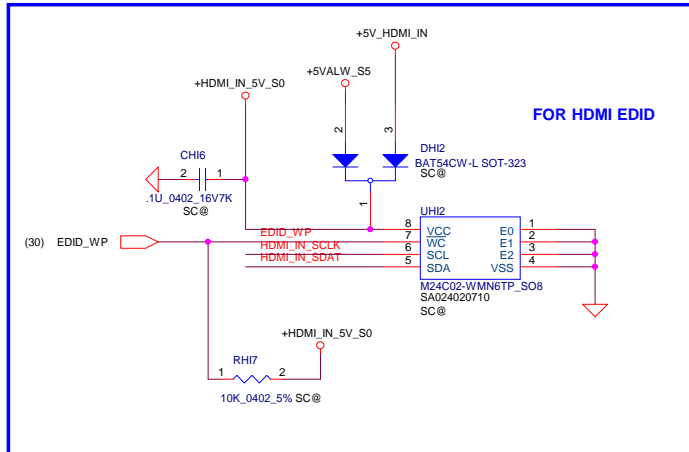
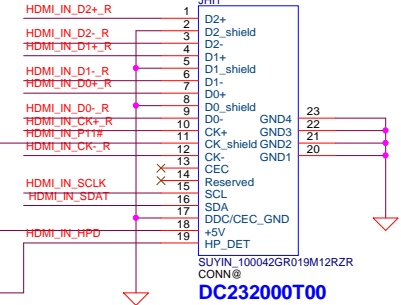
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2015/12/25	Deciphered Date	2016/09/24	Title LVDS/DMIC/CAM/Touch			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document	Number	Rev
				Custom		LA-H031P	0.1
				Date:	Tuesday, December 04, 2018	Sheet	31 of 63



0619 : CHI4 change to POP & ESD@

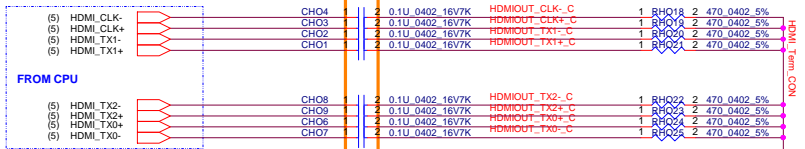
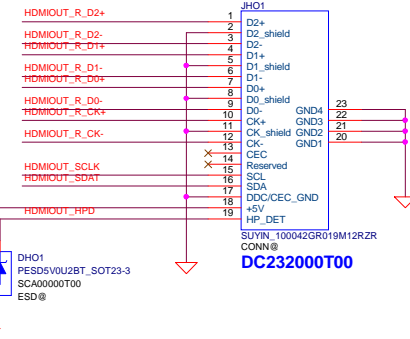
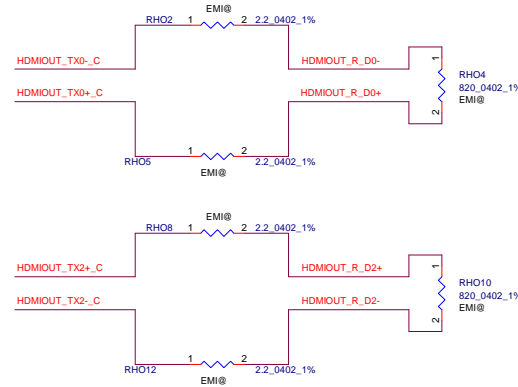
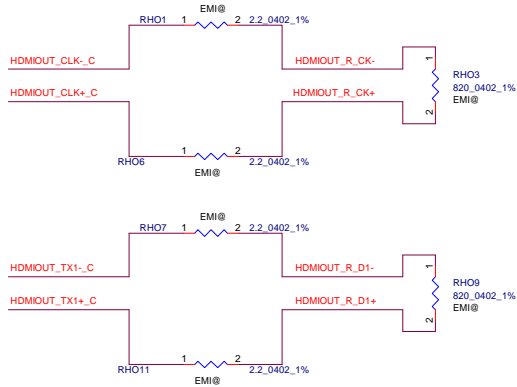


HDMI-in Connector



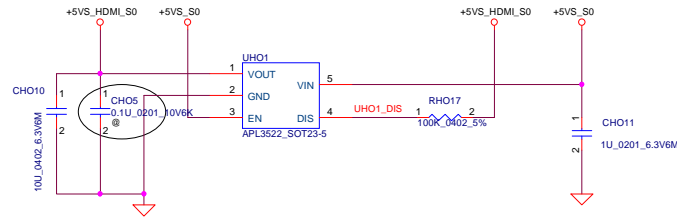
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2015/12/25	Deciphered Date	2016/09/24	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				HDMI-IN conn	
Size	Document	Number	Rev	LA-H031P	
Date:	Tuesday, December 04, 2018	Sheet	32	of 63	

1008: Remove co-layout choke LH01,LH02,LH03,LH04



Close to JHDMI2

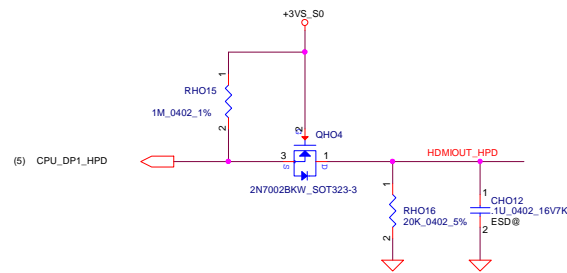
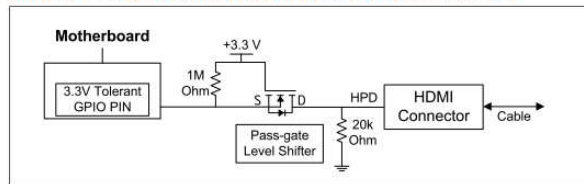
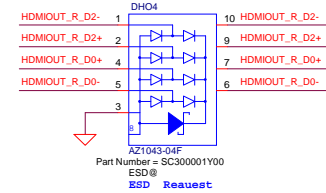
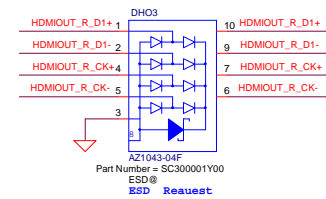
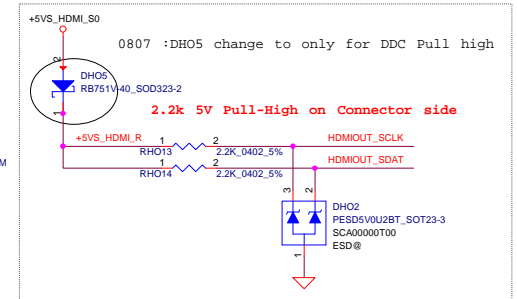
Close to JHDMI2,<1000mils Length



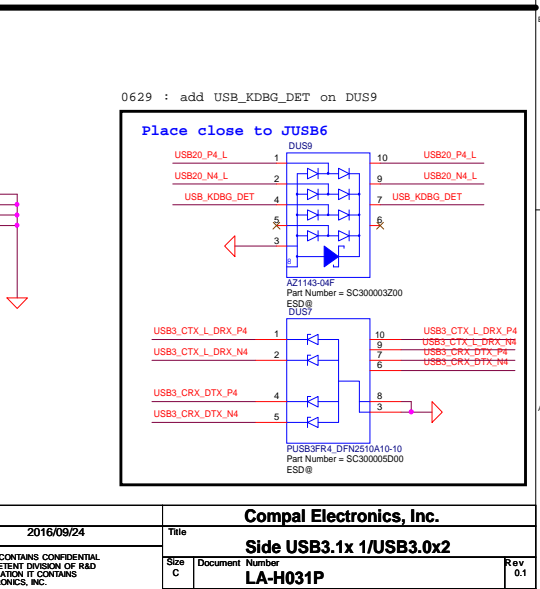
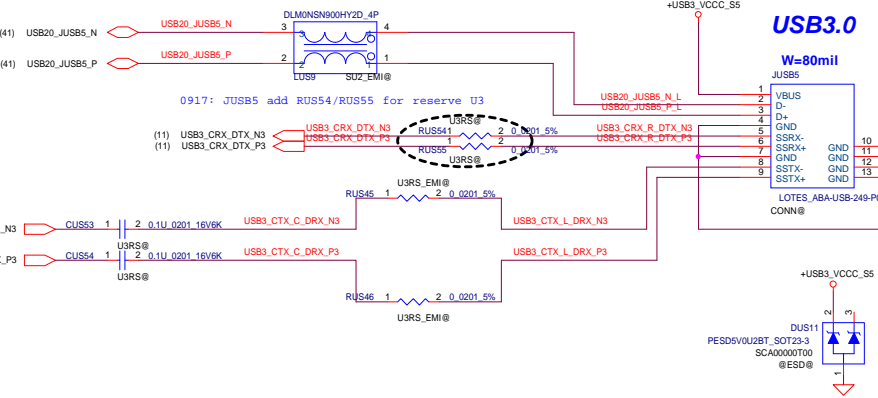
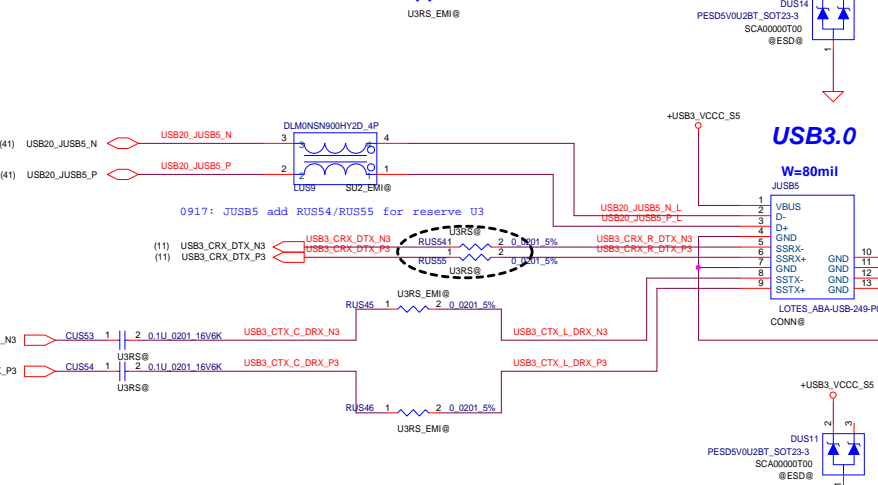
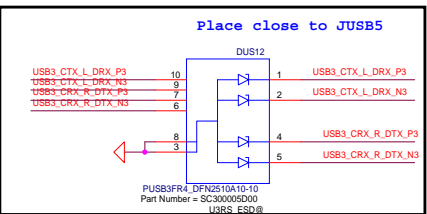
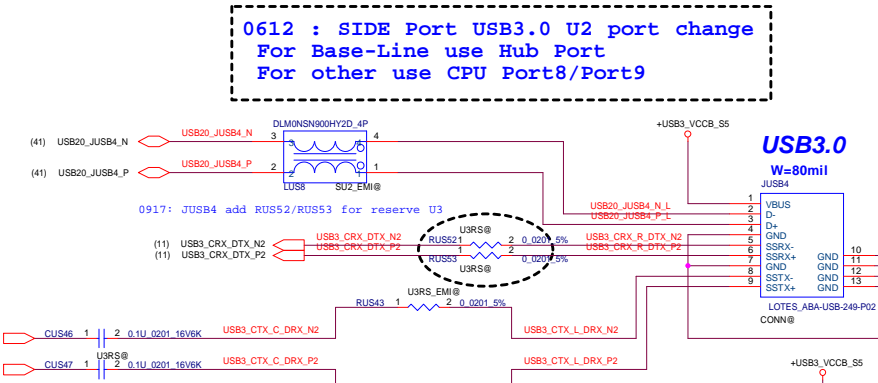
PCH Side pull
high at page 15

CONN Side pull
high at page 32

Close to JHDMI2



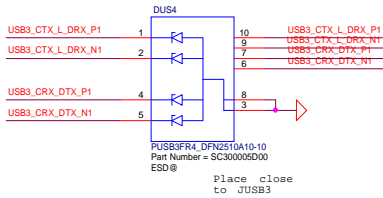
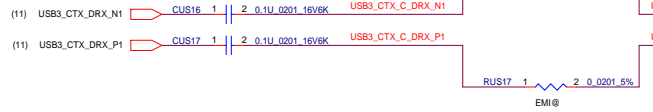
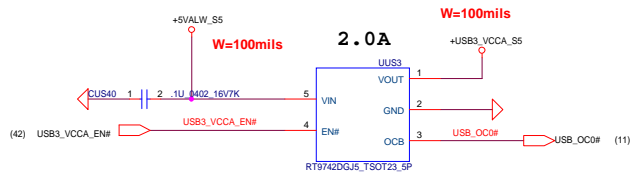
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2015/12/25	Deciphered Date	2015/10/02	Title	HDMI IN	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
					LA-H031P	0.1
				Date:	Tuesday, December 04, 2018	Sheet 33 of 63



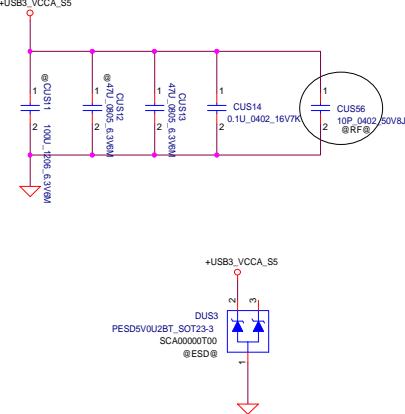
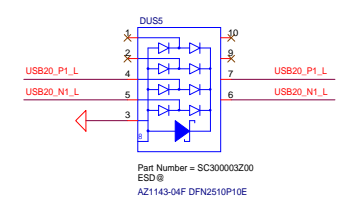
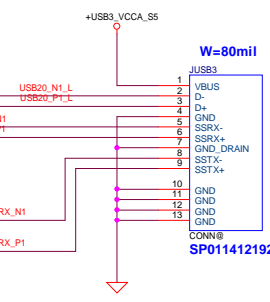
USB MUX Selection	
KDBG_MUX_SEL	Output
H	D = D2
L	D = D1

Security Classification	Compal Secret Data	
Issued Date	2015/12/25	Deciphered Date 2016/09/24
<p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND PROPRIETARY INFORMATION. THE INFORMATION HEREON MAY NOT BE TRANSFERRED FROM THE CURRENT CUSTOMER OF R&D DEPARTMENT WITHOUT PERMISSION OF COMPAL ELECTRONICS, INC. NEITHER THIS INFORMATION NOR THE INFORMATION CONTAINED HEREIN MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</p>		

Compal Electronics, Inc.			
Title			
Side USB3.1x 1/USB3.0x2			
Size	Document Number		Rev
C	LA-H031P		0.1
Date	Tuesday, December 04, 2018	Sheet	34 of 63



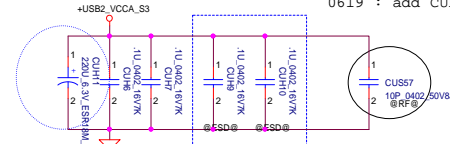
Rear USB3.1 GEN2



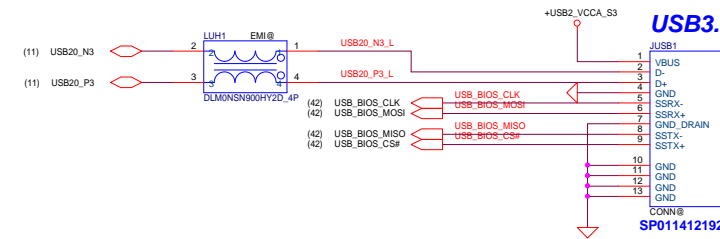
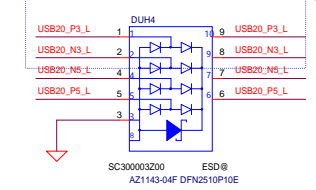
No support BIOS recovery, EC debug only

0627 : CUH11 change SIZE

0619 : add CUH9/CUH10 for ESD



0628: Swap DUH4 Pin1/Pin2 , Pin8/Pin9



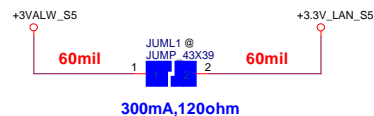
USB3.0 Conn.

SP011412192

USB2.0 Conn.

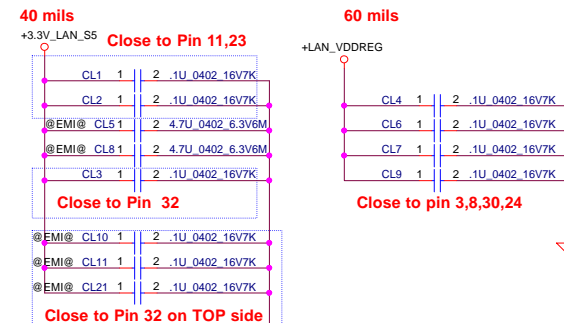
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/12/25	Deciphered Date	2016/09/24	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSMITTED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RAD DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Rear USB3.1x1 / USB2.0 x2
Size C	Document Number	LA-H031P	Sheet 35 of 63	Rev 0.1
Date:	Tuesday, December 04, 2016			

WOL circuit (Connect +3V_LAN to +3VALW)



+3V_LAN rising time (10%~90%) need > 0.5ms and <100ms.

Power (Decoupling Cap.)

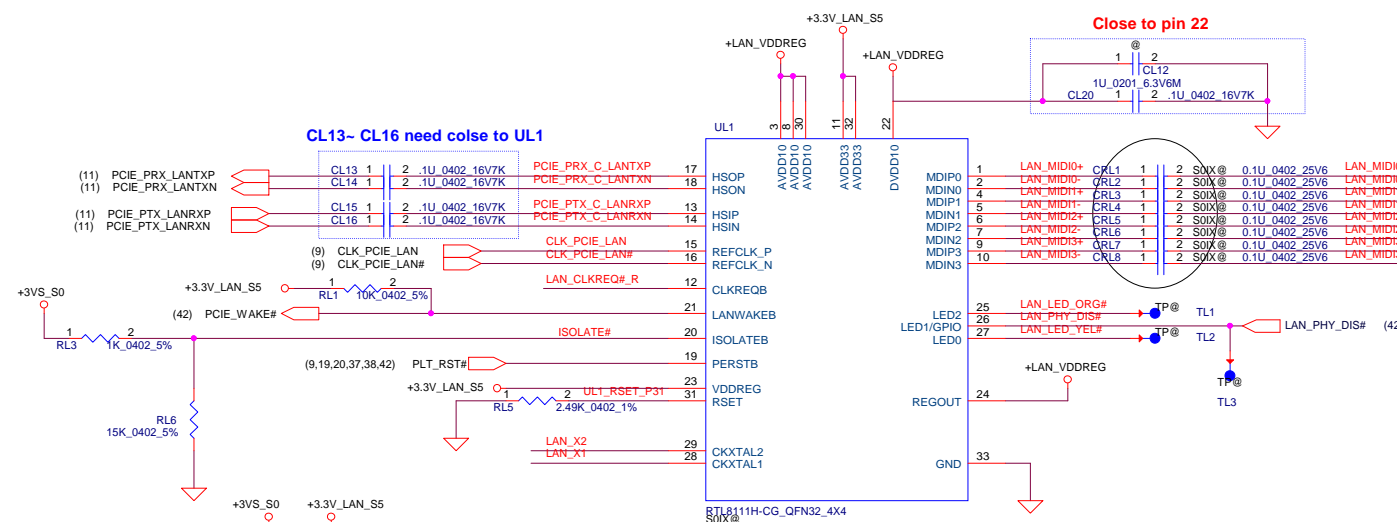
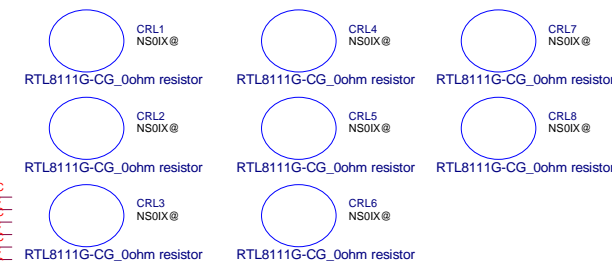


LED Status

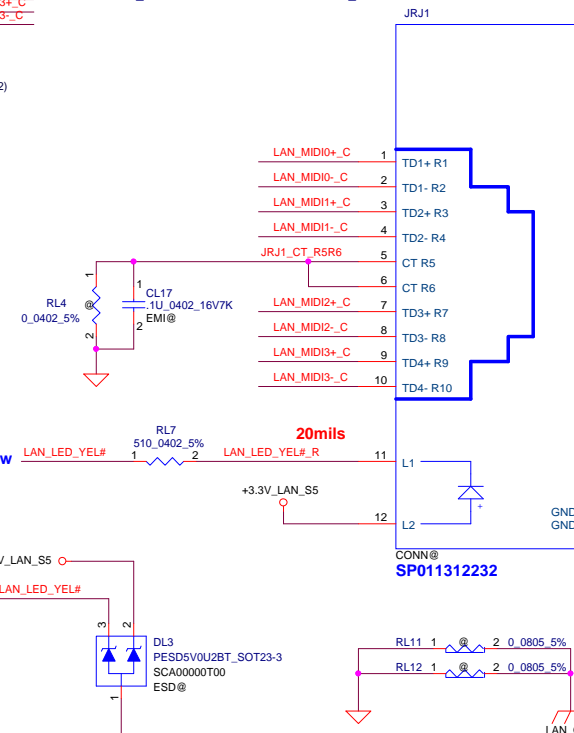
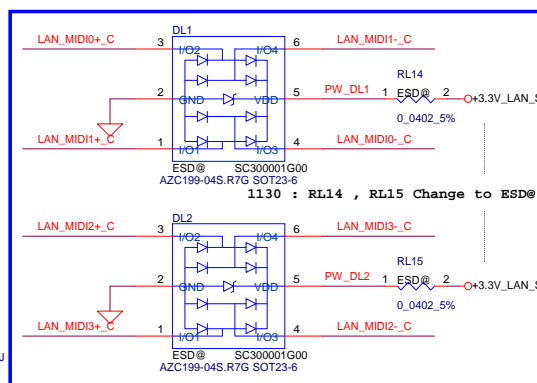
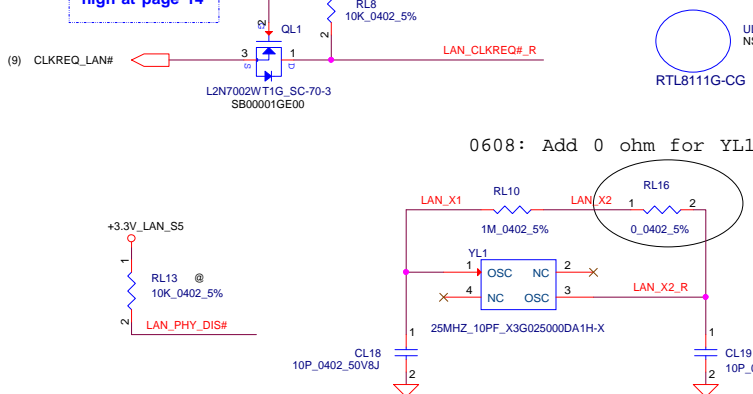
WOL	status	Yellow
don't care	No Link	off
off(ME WOL and Host WOL should be disable both)	S3/S4/S5	off
on	10M,inactive	
on	10M,active	
on	100M,inactive	
on	100M,active	
on	1G,inactive	
on	1G,active	

always on
blinking

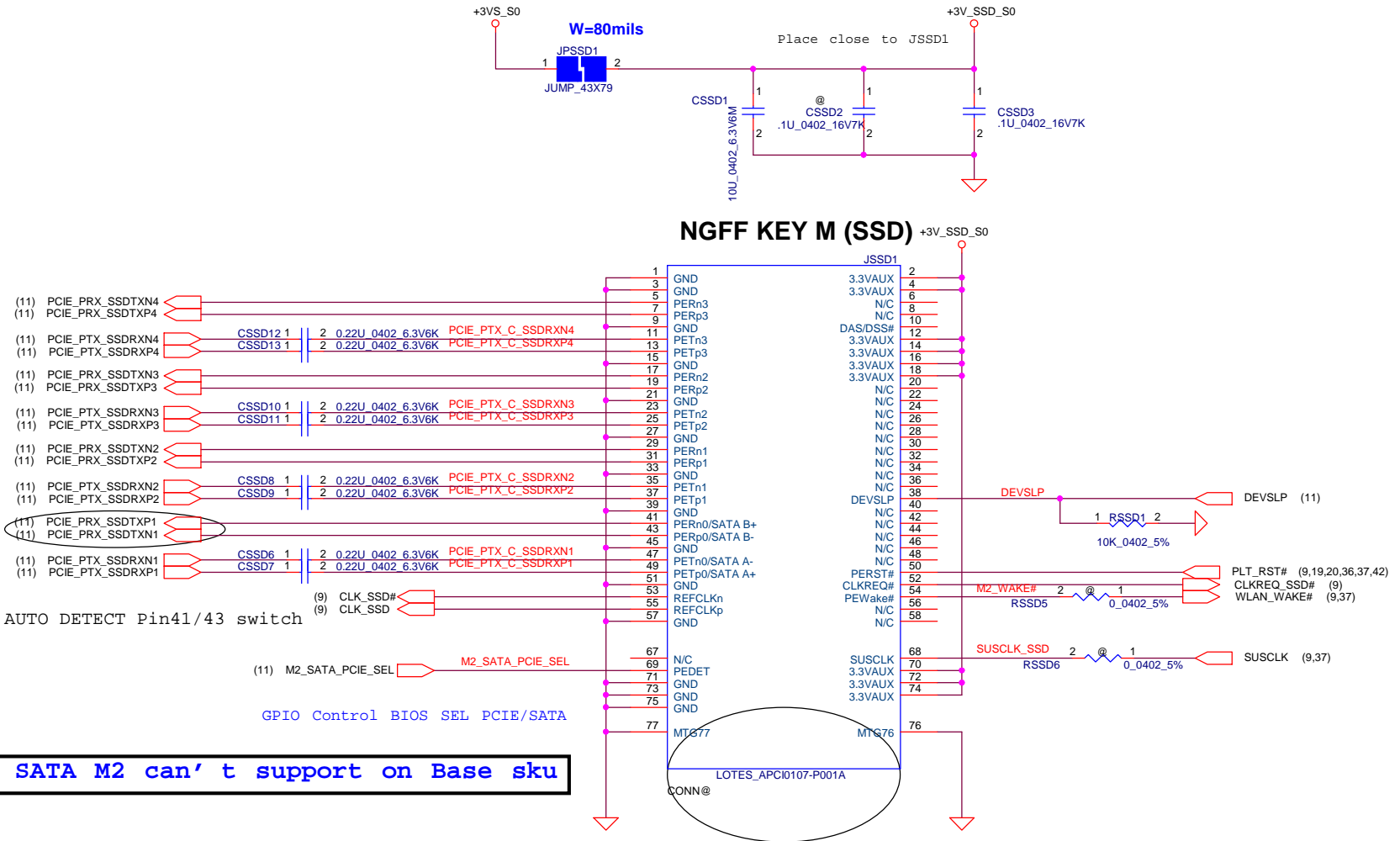
8111G resistor/8111H capacitor



8111G/8111H LAN chip

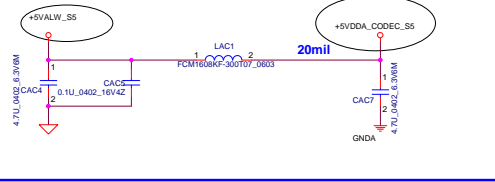




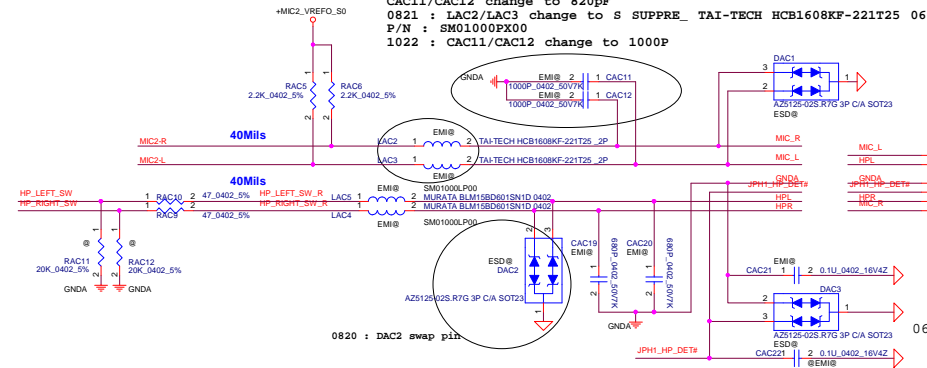


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/12/25	Deciphered Date	2013/09/01	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				SSD (M2)	
				Size B	Document Number
				LA-H031P	
Date: Tuesday, December 04, 2018				Sheet	38 of 63

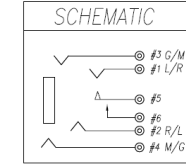
0611: AVDD1 change to S5 power



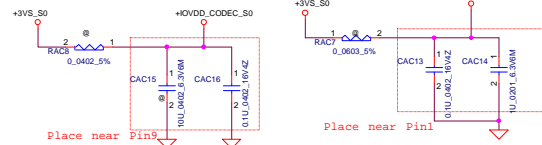
0820 : LAC2/LAC3 change to BLM18KG221SN1D_2P (0603)
CAC11/CAC12 change to 820pF
0821 : LAC2/LAC3 change to S SUPPRE_TAI-TECH HCB1608KF-221T25 0603
P/N : SM01000PX00
1022 : CAC11/CAC12 change to 1000P



Combo JACK



0607: Change JHP1 (Correct Symbol Pin define)



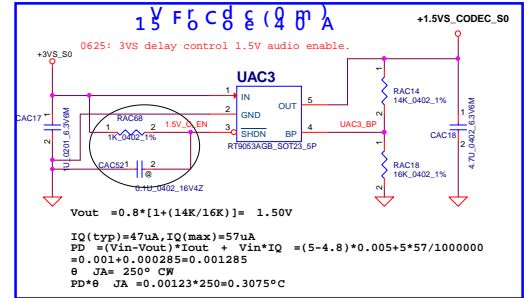
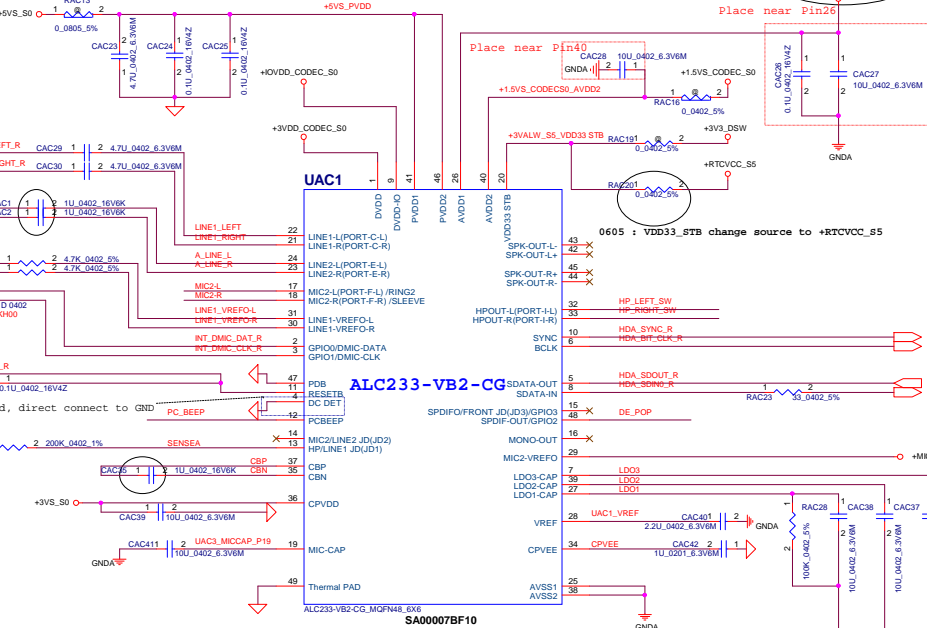
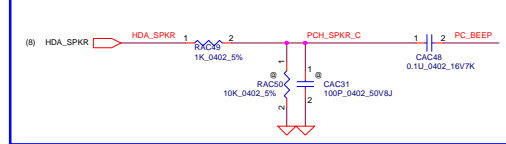
0612 : CAC1/CAC2/CAC35 change 0402

0703: LAC6 change to SM01000KH00
CAC33 change to pop

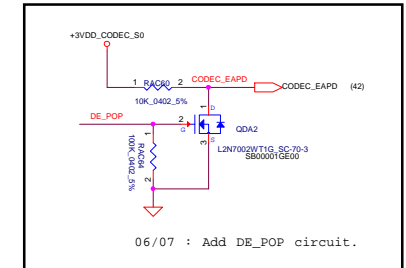
0619 : CAC33 change to 220P & CAC33/CAC51 change to unpop



PC Beep

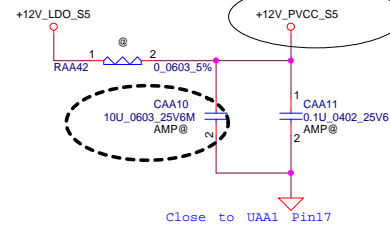
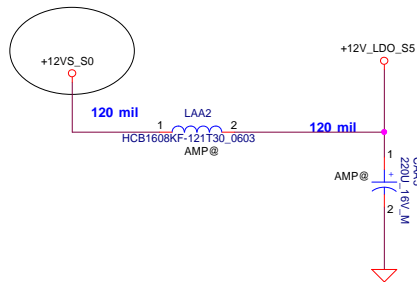


0625: 3VS delay control 1.5V audio enable.
Vout = 0.8 * [1 + (14K/16K)] = 1.50V
IQ(typ) = 47uA, IQ(max) = 57uA
PD = (Vin - Vout) * Iout + Vin * IQ = (5 - 4.8) * 0.005 + 5 * 57 / 1000000
= 0.001 + 0.000285 = 0.001285
θ JA = 250° C/W
PD * θ JA = 0.00123 * 250 = 0.3075°C



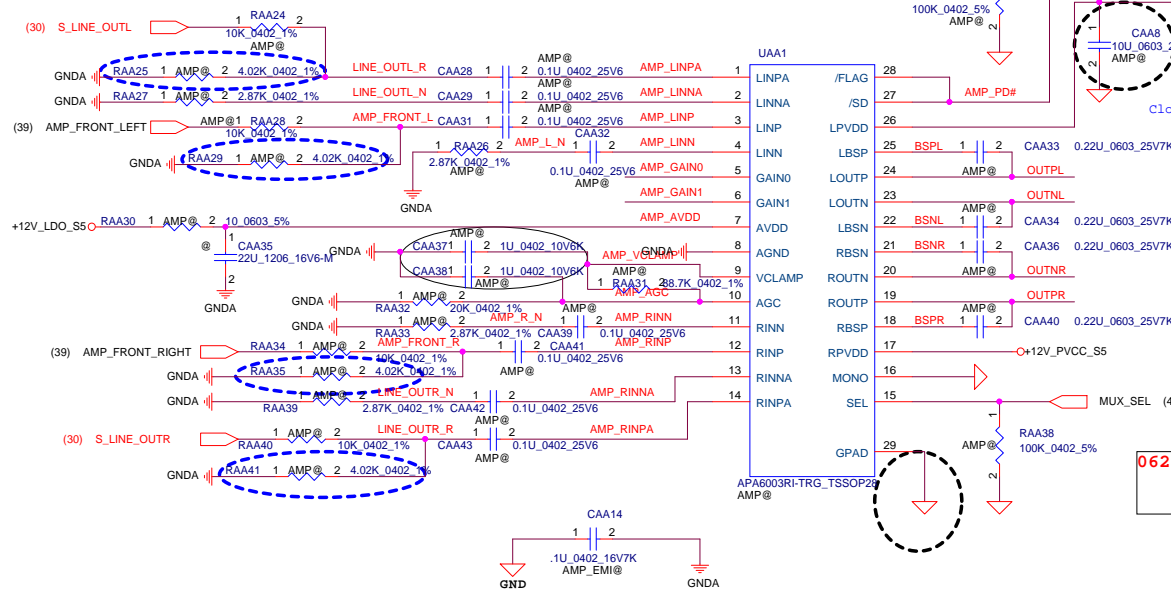
0607 : Add DE_POP circuit.

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	
2014/09/24		2016/09/24		HDA Audio Codec ALC233-VC	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSMITTED FROM THE CUSTODY OF THE COMPETENT DIVISION OF HAD DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Rev		Rev	
8256		Document Number		LA-H031P	
Customer		Date: Tuesday, December 04, 2018		Sheet 39 of 83	



0917 : CAA10/CAA8 change to SE0000X200 S CER CAP 10U 25V M X5R 0603

0821 : RAA25 / RAA29 / RAA35 / RAA41 for test result change to 4.02K

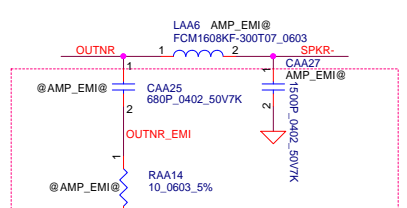
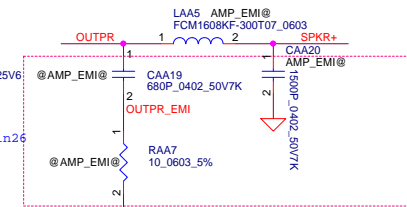
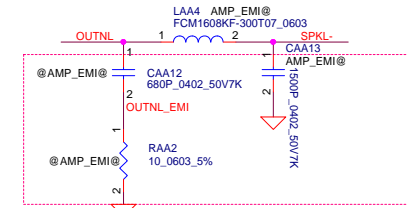
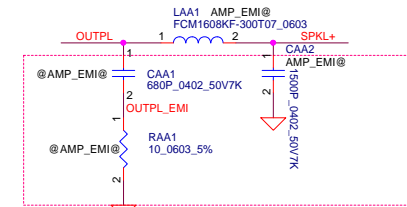
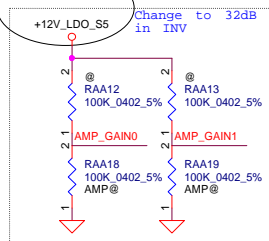


0821 : GPAD change to GND

MUX_SEL	L=Audio Codec Input source H=Scalar Input source
---------	---

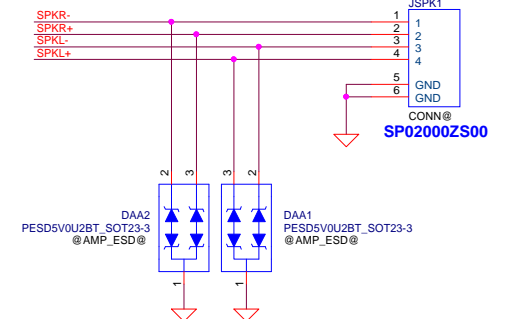
GAIN1	GAIN0	AV (inv)	INPUT IMPEDANCE
0	0	20dB	60Kohm
0	1	26dB	30Kohm
1	0	32dB	15Kohm
1	1	36dB	9Kohm

APA6003 for Speaker (CRB)



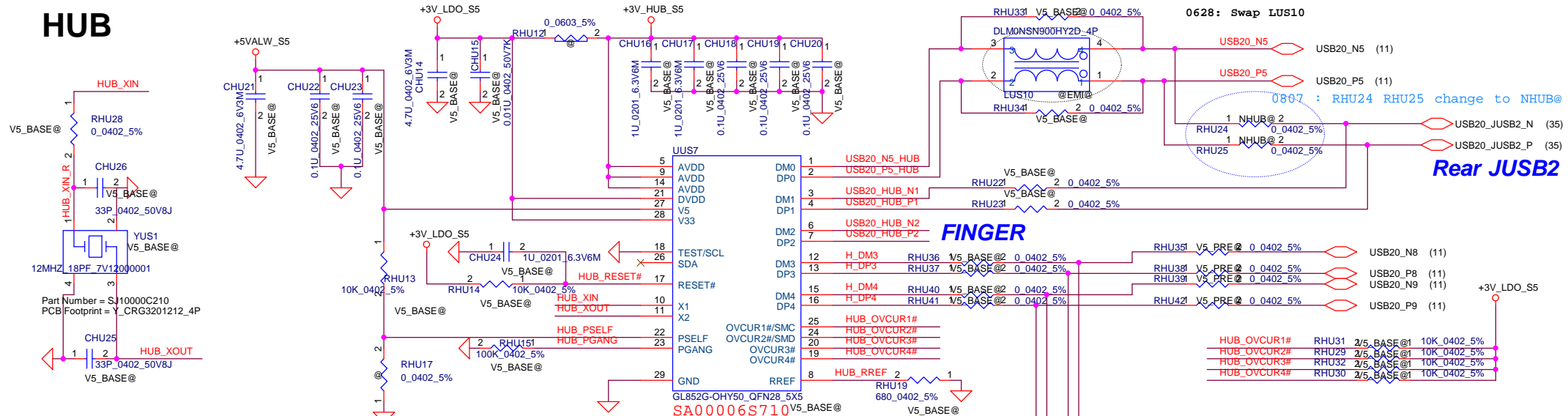
0626 : CAA2/CAA13/CAA20/CAA27 change to AMP_EMI@ 0402 type
CAA1/CAA12/CAA19/CAA25 change to 0402 type
RAA1/RAA2/RAA7/RAA14 change to 0603 type

Speaker Conn.
3Wx2 4ohm Speaker



Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2015/12/25		Deciphered Date		2016/12/15		Title			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						Amp ANPEC APA6003					
						Size		Document Number		Rev	
						Custom		LA-H031P		0.1	
						Date:		Tuesday, December 04, 2018		Sheet 40 of 63	

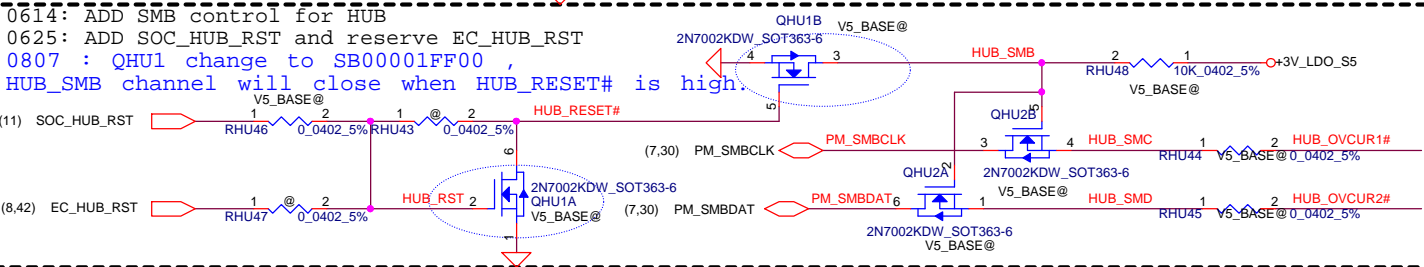
HUB



Rear JUSB2

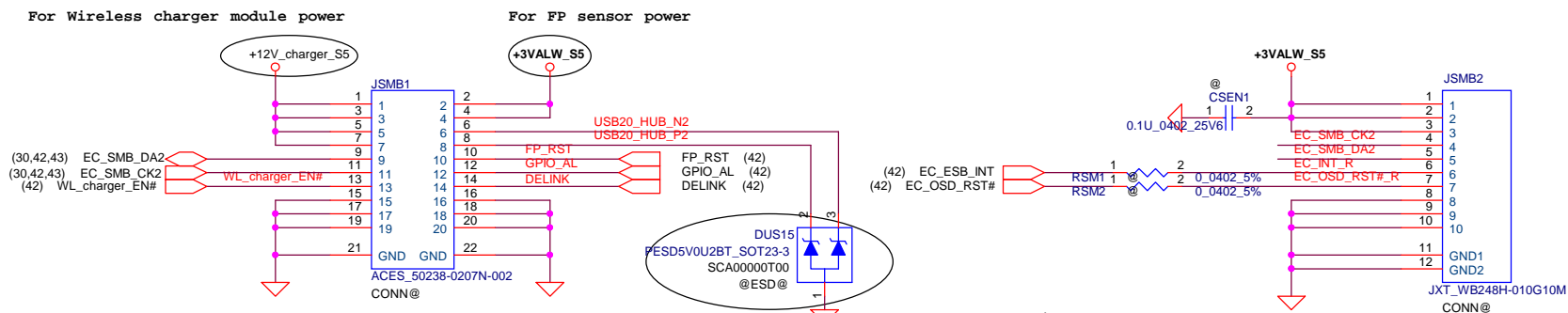
FINGER

```
0614: ADD SMB control for HUB
0625: ADD SOC_HUB_RST and reserve EC_HUB_RST
0807 : QHU1 change to SB00001FF00 ,
HUB_SMB channel will close when HUB_RESET# is high.
```



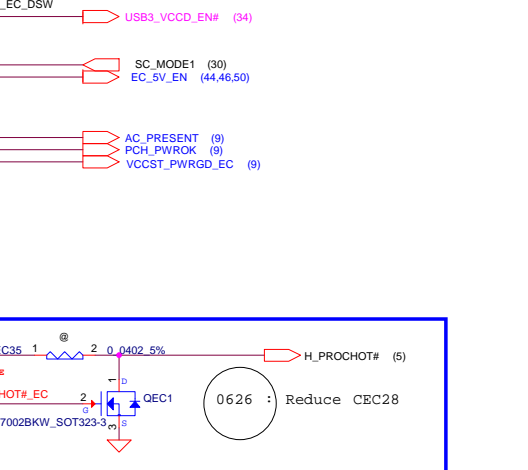
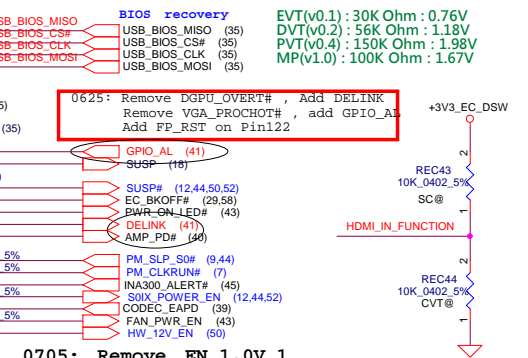
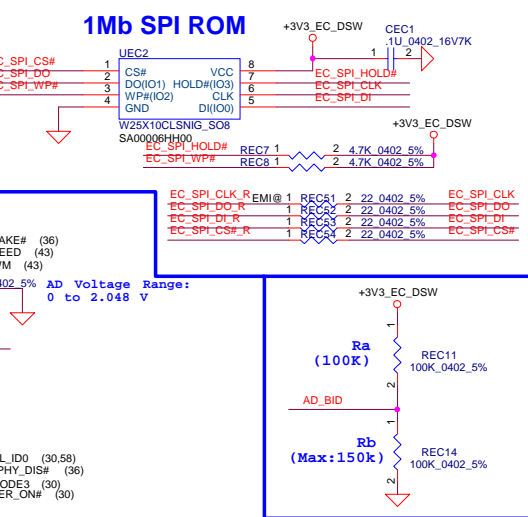
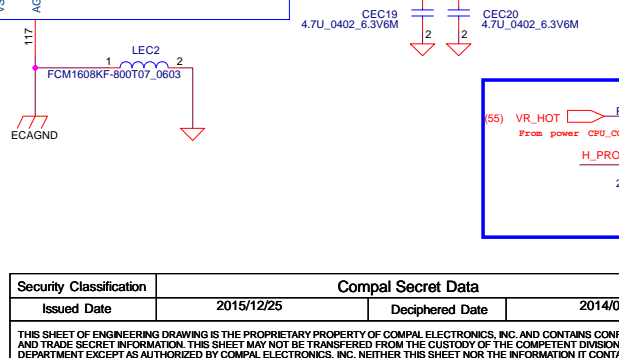
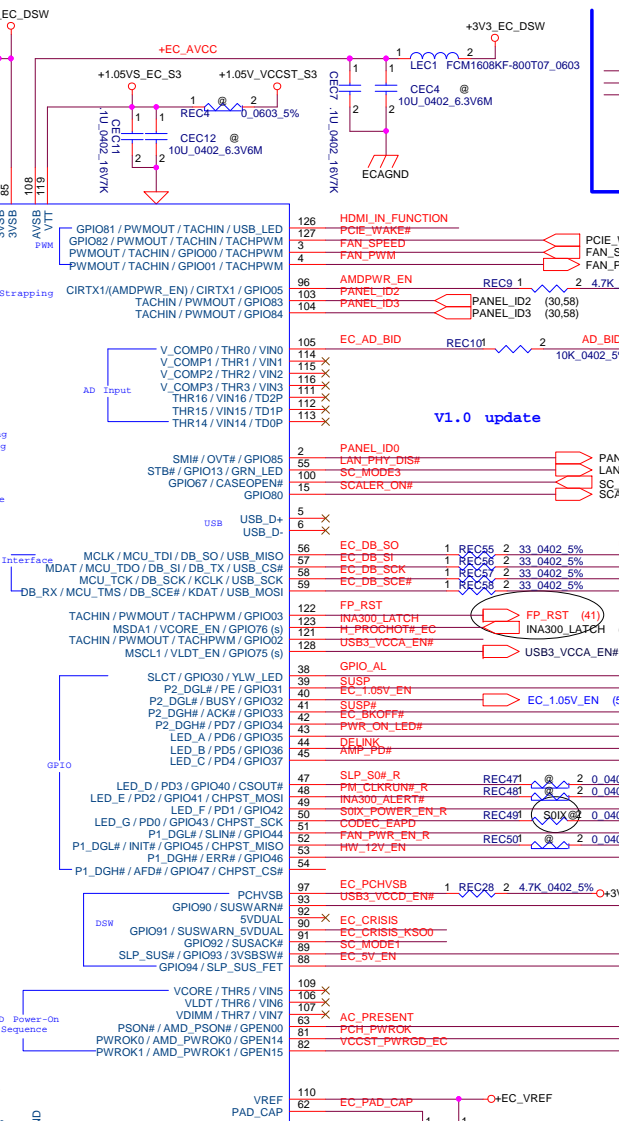
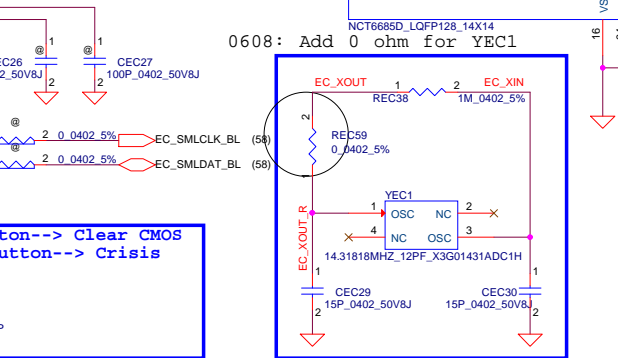
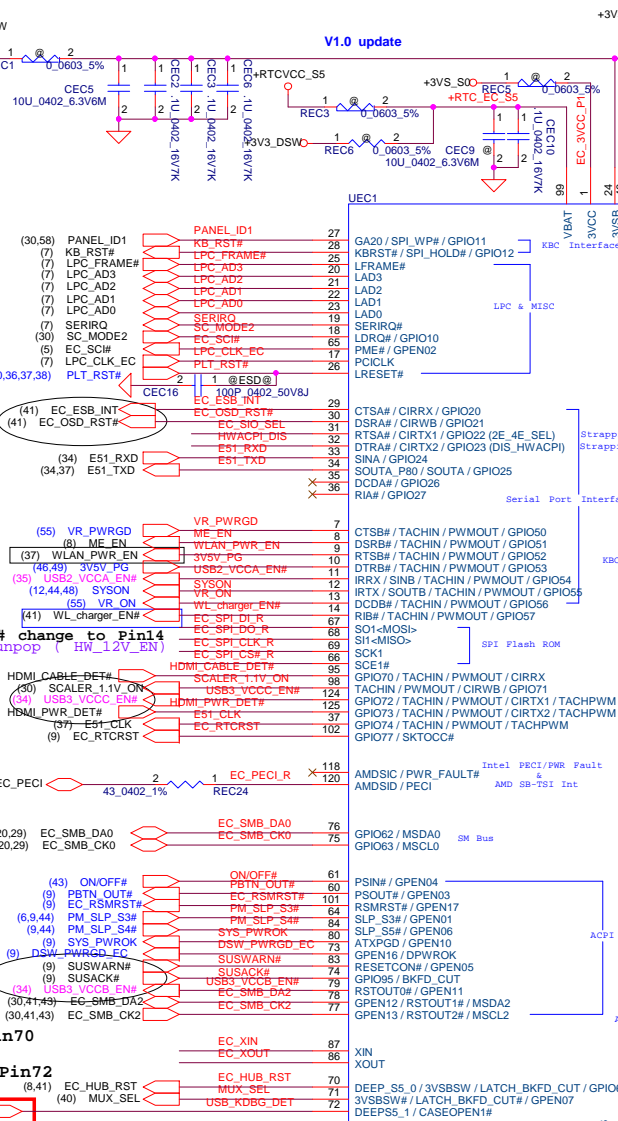
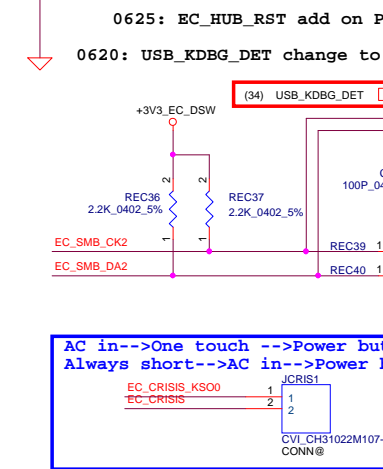
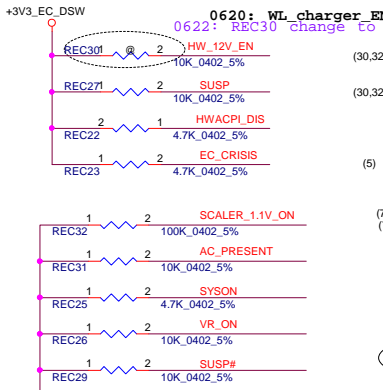
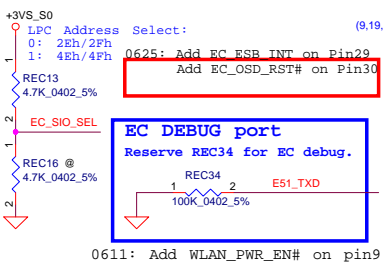
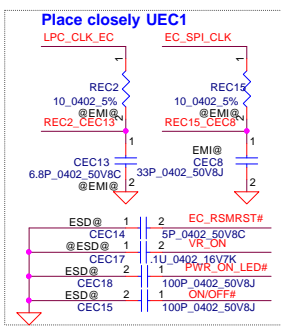
SMB Function CONN. (20pin)

FOR CAP SENSOR CONN. (10pin)



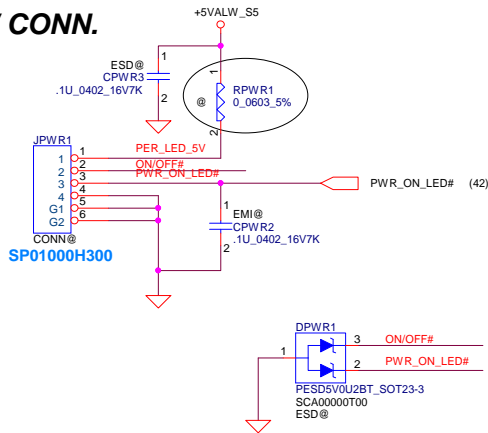
```
0627 : ADD ESD Diode on JSMB1
```

Security Classification		Compal Secret Data		Compal Electronics, Inc. SMB Function (Reserve)		
Issued Date	2015/12/25	Deciphered Date	2015/10/02	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				LA-H031P		0.1
Date:				Tuesday, December 04, 2018	Sheet	41 of 63

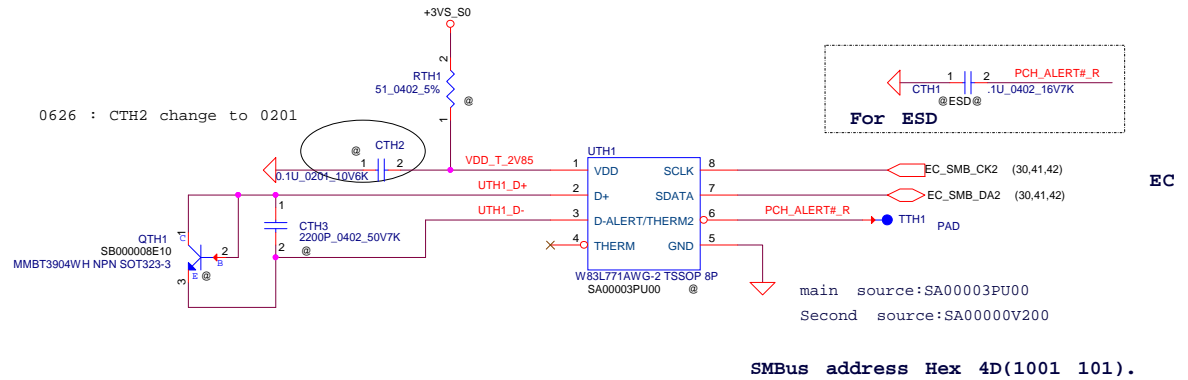


Security Classification		Compal Secret Data		Title	
Issued Date	2015/12/25	Deciphered Date	2014/04/01	EC NCT6685	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Size		Document Number	Rev
		Custom		LA-H031P	0.1
		Date:		Tuesday, December 04, 2018	Sheet 42 of 63

Power SW CONN.

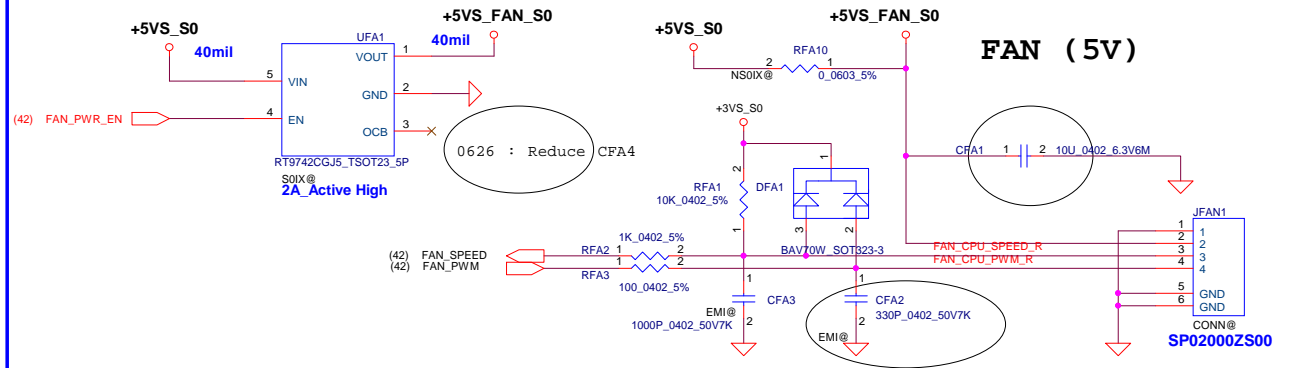
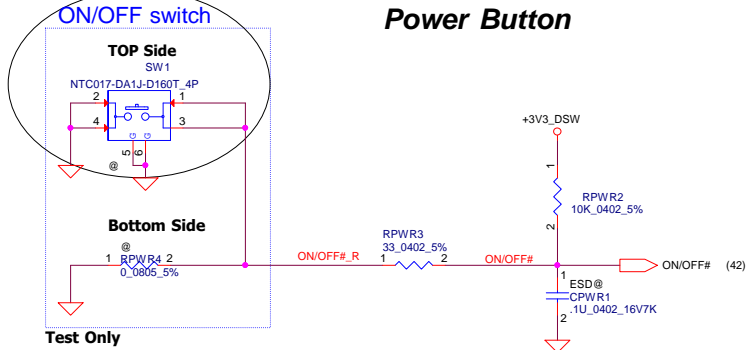


Thermal Sensor



1122 : SW1 change to unpop

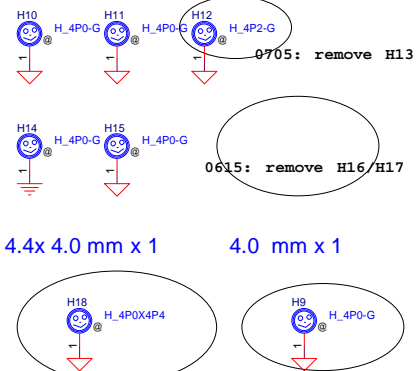
Power Button



PCB Screw Hole

4.0 mm x 8

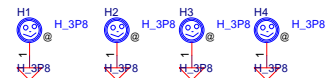
0815 : H12 change to 4P2



0810 : H9 change to 4P0
0815 : H18 change to H_4P0X4P4

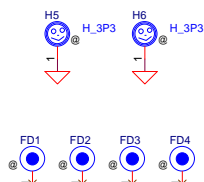
CPU Hole

3.8mm x 4



GPU Hole

3.3 mm x 2

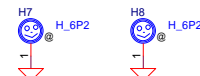


WIFI Hole



SSD Hole

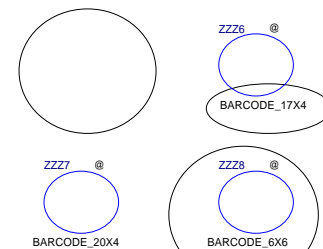
6.2 mm x 2



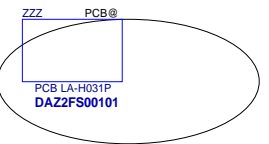
BARCODE

0822 : ZZZ6 change to 17x4 (DFB)

1012 : Remove BARCODE_8x8



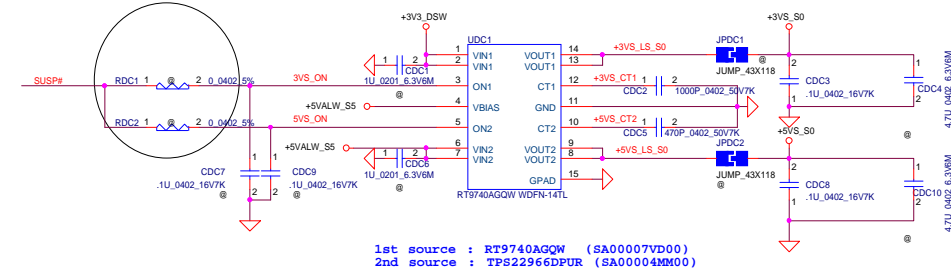
1008 : Barcode 10x10 change to 6x6



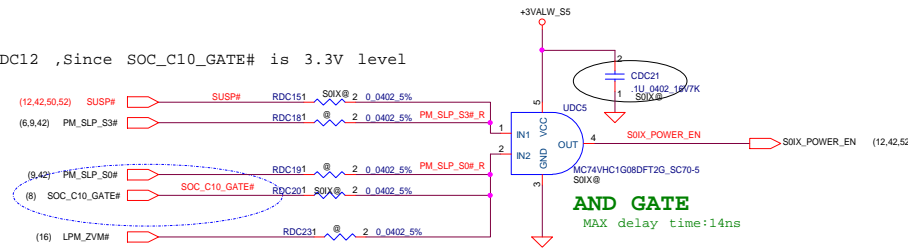
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/12/25	Deciphered Date	2016/09/24	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PWR SW/THERMAL/FAN/SCREW	
Size	Custom	Document Number	LA-H031P	Rev	0.1
Date: Tuesday, December 04, 2018		Sheet		43 of 63	

VIN 5V and 3.3V (VBIA5=5V),IMAX(per channel)=6A,Rds=18mohm

1122 : RDC1/RDC2 change to shortpad

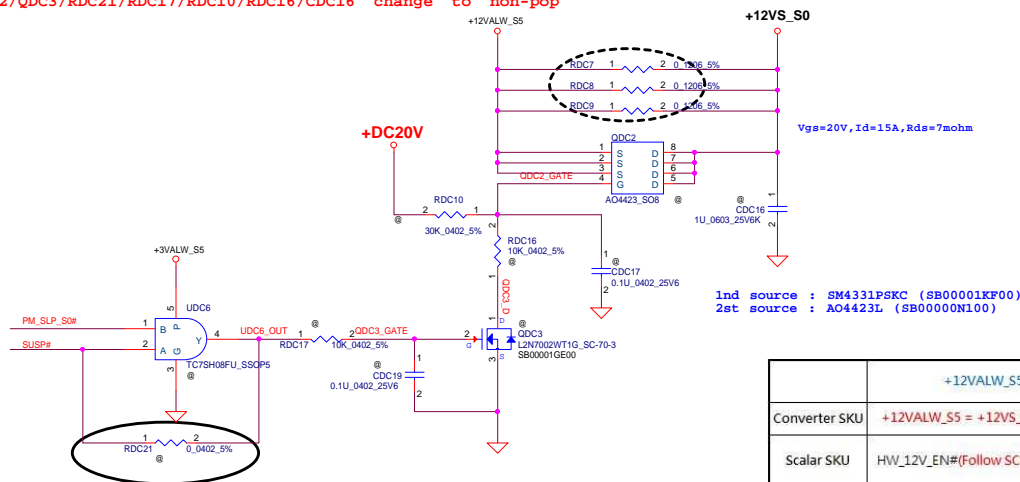


0801: Delete QDC4/RDC22/RDC12 ,Since SOC_C10_GATE# is 3.3V level

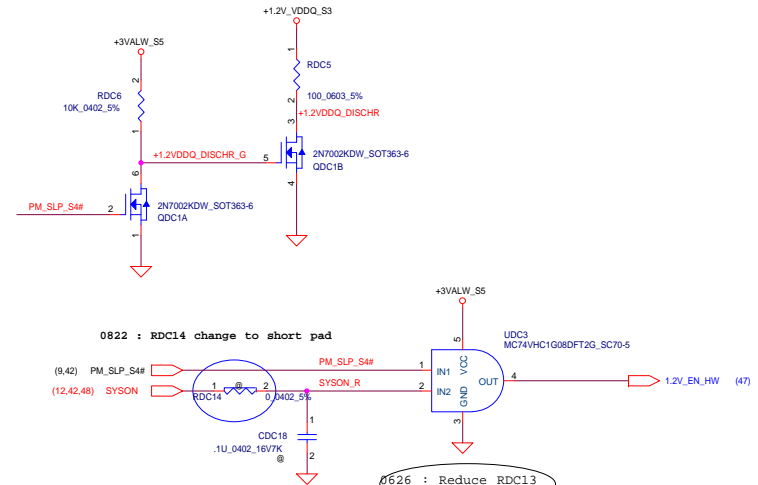
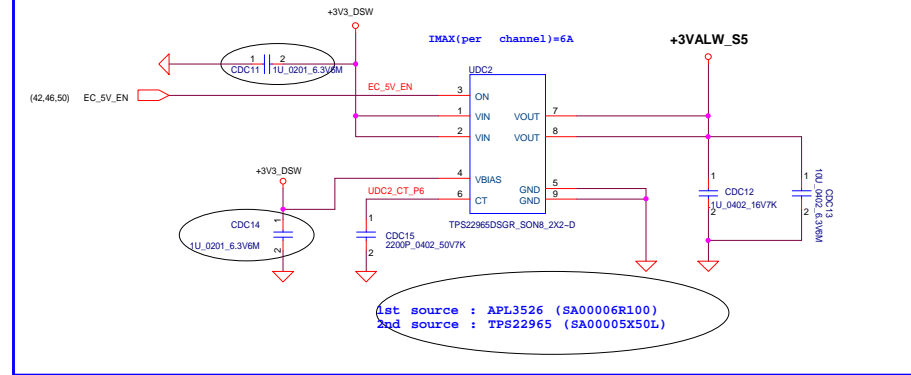


+12VALW_S5 TO +12VS_S0 (PMOS)

0827 : RDC7/RDC8/RDC9 change to all SKU pop
QDC2/QDC3/RDC21/RDC17/RDC10/RDC16/CDC16 change to non-pop



+3VDSW_S5 to +3VALW_S5 Transfer

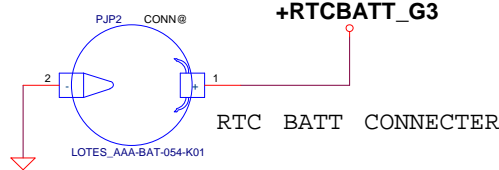


	+12VALW_S5	+12VS_S0	BOM
Converter SKU	+12VALW_S5 = +12VS_S0 , Enable: HW_12V_EN# (Follow SPL_S3#)		RDC7,RDC8,RDC9
Scalar SKU	HW_12V_EN#(Follow SCALAR_ON#)	SUSP# (Follow SPL_S3#)	QDC2,RDC10,RDC16,RDC17,CDC19,CDC17

+3VL_S5

PR17
0.0402_5%

+3VL_RTC_S5



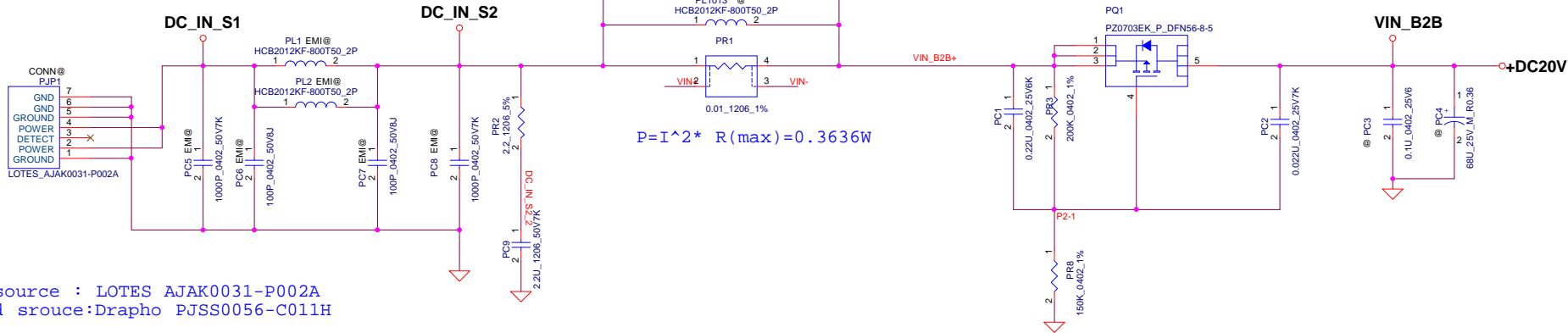
tekni-indonesia.com

W/O INA300 : PL1012, PL1013 pop
W/ INA300: PR1 pop

Main source: PZ0703EK
 $PD = I^2 \cdot R_{ds(on)} = 6^2 \cdot 7m \text{ ohm} = 0.252W$
 $\theta \text{ JA} = 50^\circ \text{ C/W} \cdot 0.252W = 12.6^\circ \text{ C}$

Second source: AON6405L
 $PD = I^2 \cdot R_{ds(on)} = 6^2 \cdot 7m \text{ ohm} = 0.252W$
 $\theta \text{ JA} = 50^\circ \text{ C/W} \cdot 0.252W = 12.6^\circ \text{ C}$

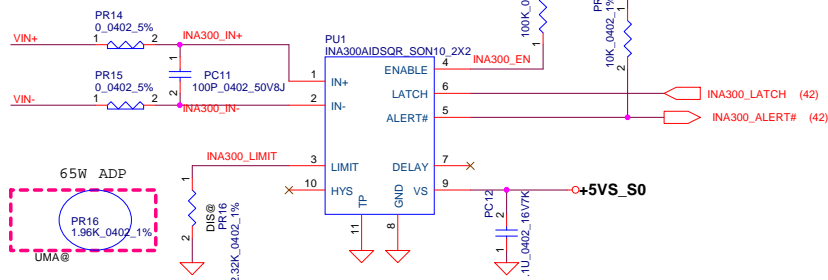
Third source: SIR403EDP-T1-GE3
 $PD = I^2 \cdot R_{ds(on)} = 6^2 \cdot 6.5m \text{ ohm} = 0.234W$
 $\theta \text{ JA} = 65^\circ \text{ C/W} \cdot 0.468W = 15.21^\circ \text{ C}$



main source : LOTES AJAK0031-P002A
second srouce: Drapho PJSS0056-C011H

+3VS_S0

Current Limit Function

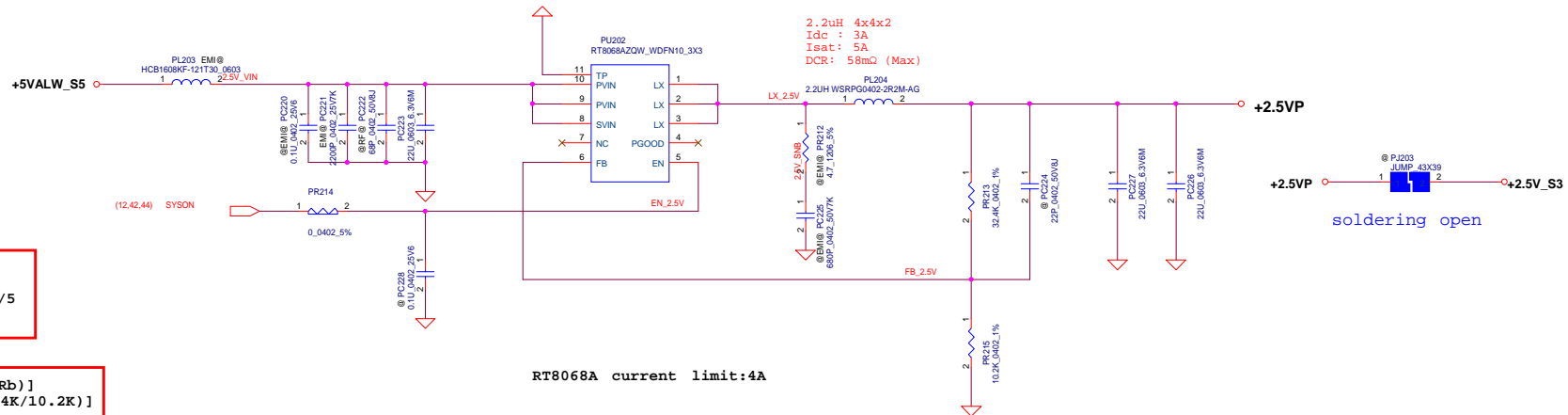


UMA 65W:
Full Load(100%) --> 3.25A
 $V_{trip} = 3.25 \cdot 10m = 32.5mV$
 $V_{Limit} = V_{trip}; R_{Limit} = (32.5mV + 0.5mV) / 20uA = 1.65K$
Trigger(120%) --> 3.9A (@78W)
 $V_{trip} = 3.9 \cdot 10m = 39mV$
 $R_{Limit} = (39mV + 0.5mV) / 20uA = 1.975K$
Select $R_{Limit} = 1.96K$
 $I_{Trigger} \rightarrow 3.87A$

DIS 90W:
Full Load(100%) --> 4.5A
 $V_{trip} = 4.5 \cdot 10m = 45mV$
 $V_{Limit} = V_{trip}; R_{Limit} = (45mV + 0.5mV) / 20uA = 2.275K$
Trigger(116.7%) --> 5.25A (@105W)
 $V_{trip} = 5.25 \cdot 10m = 52.5mV$
 $R_{Limit} = (52.5mV + 0.5mV) / 20uA = 2.65K$
Select $R_{Limit} = 2.61K$
 $I_{Trigger} \rightarrow 5.22A$

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/12/18	Deciphered Date	2013/12/18	Title DCIN / CONN	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number Rev 0.1
Date: Tuesday, December 04, 2018				Sheet 45	of 63


```
1st source : RT8068AZQW
2nd srouce : UP1727PDDA
3rd source : GS7302ADTD-R
```



+2.5VP
 $V_{in} = 5V$
 $I_{in} = 2.5 \cdot 0.5 / 0.85 / 5$
 $= 0.29A$

$$\begin{aligned} V_{out} &= V_{fb} \cdot [1 + (R_t/R_b)] \\ &= 0.6 \cdot [1 + (32.4\text{K}/10.2\text{K})] \\ &= 2.505\text{V} \end{aligned}$$

```
+2.5VP
Ipeak=0.5A; Fsw=1MHz
ILimit=4A
Iin_ripple=0.18A
Delta_IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=0.568A
LIR=Delta_IL/IL/ripple=1.136
Cout=[L*(Iout+Delta_IL/2)^2]/[(Vout+Delta_V)^2-Vout^2]
=3.5uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.18uF
```

RT8068A current limit:4A

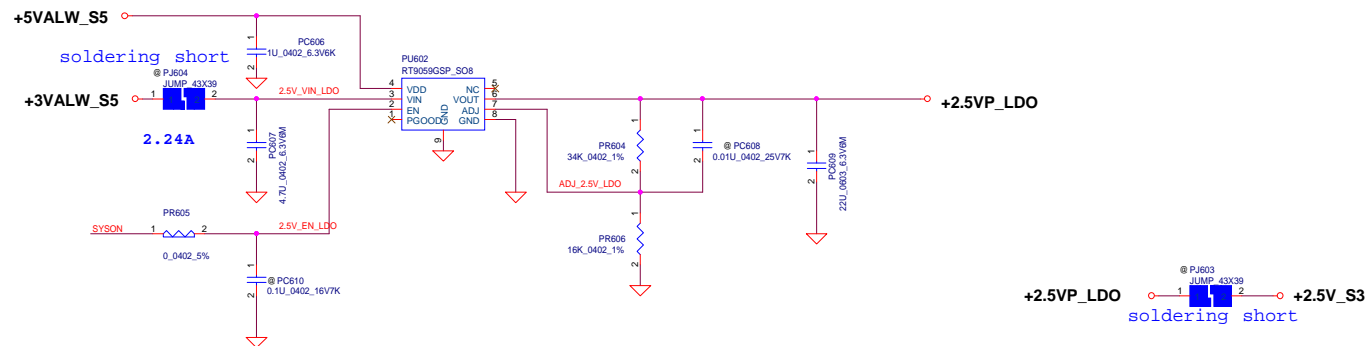
```
1st source : RT9059GSP
2nd srouce : APL5933CKAI
```

Vo	2.5	V
Vin	3.3	V
Io	0.5	A
PD	0.402	W
$\theta_{JA}(\text{main})$ $\theta_{JA}(\text{2nd})$	33.7 50	$^{\circ}\text{C/W}$

$$\begin{aligned} V_{out} &= V_{fb} \cdot [1 + (R_t/R_b)] \\ &= 0.8 \cdot [1 + (34K/16K)] \\ &= 2.5V \end{aligned}$$

```
+2.5Vp
Imax=0.35, Ipeak=0.5A
Current Limit=3.6A(Typ)~4.2A(Max)

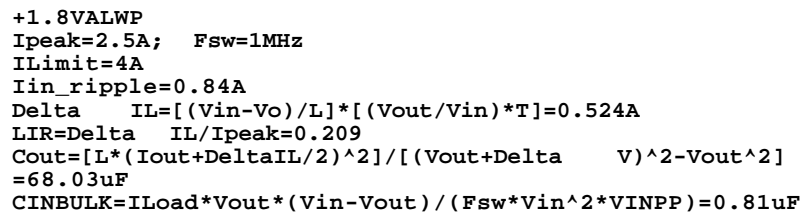
RT9059:
Quiescent Current (GND Current)
IQ(typ)=0.6mA, IQ(max)=1.2mA
PD=(Vin-Vout)*Iout+Vin*IQ=0.402W
PD*θ JA=0.402W*33.7°C/W=13.55°C
```



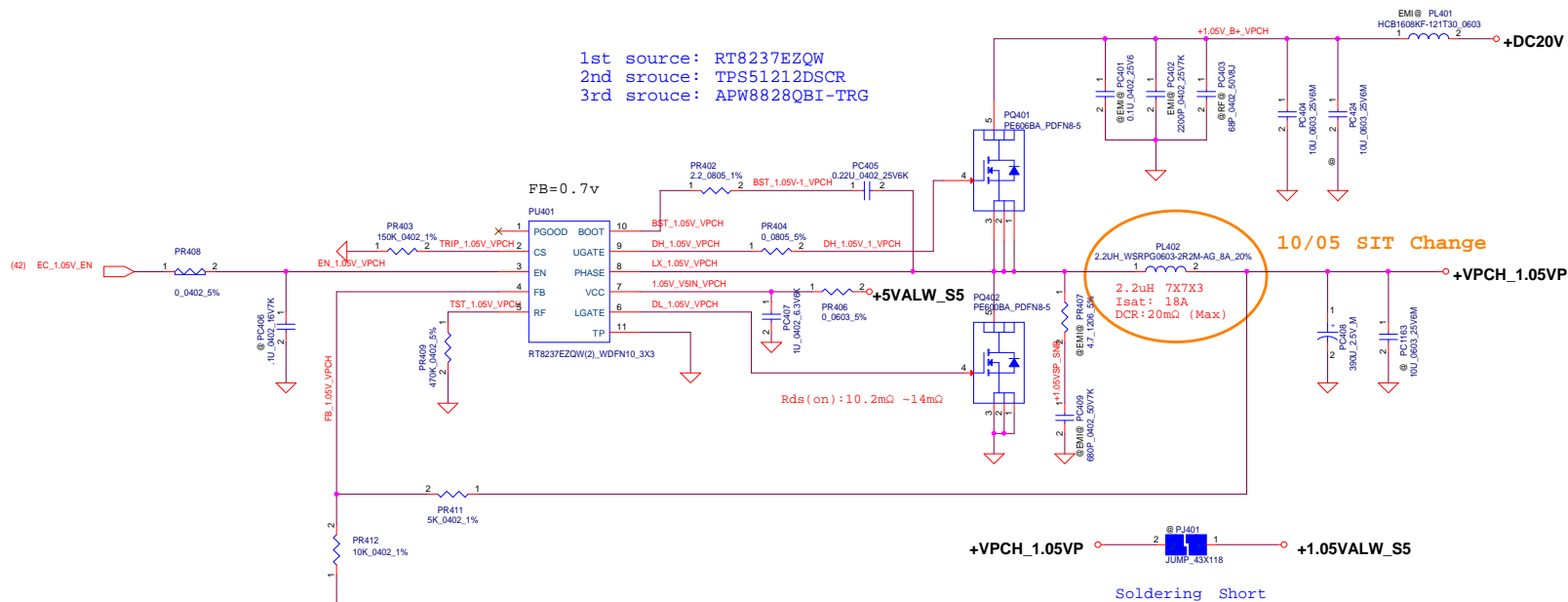
+2.5VP_LDO  **+2.5V_S3**
soldering short

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2013/08/15	Deciphered Date	2013/08/29	Title	2.5VP(RT8068A/RT9059GSP)	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev 0.1
				Date:	Tuesday, December 04, 2018	Sheet 48 of 63

2.2uH 4x4x2
Idc : 3A
Isat: 5A
DCR: 58mΩ (Max)



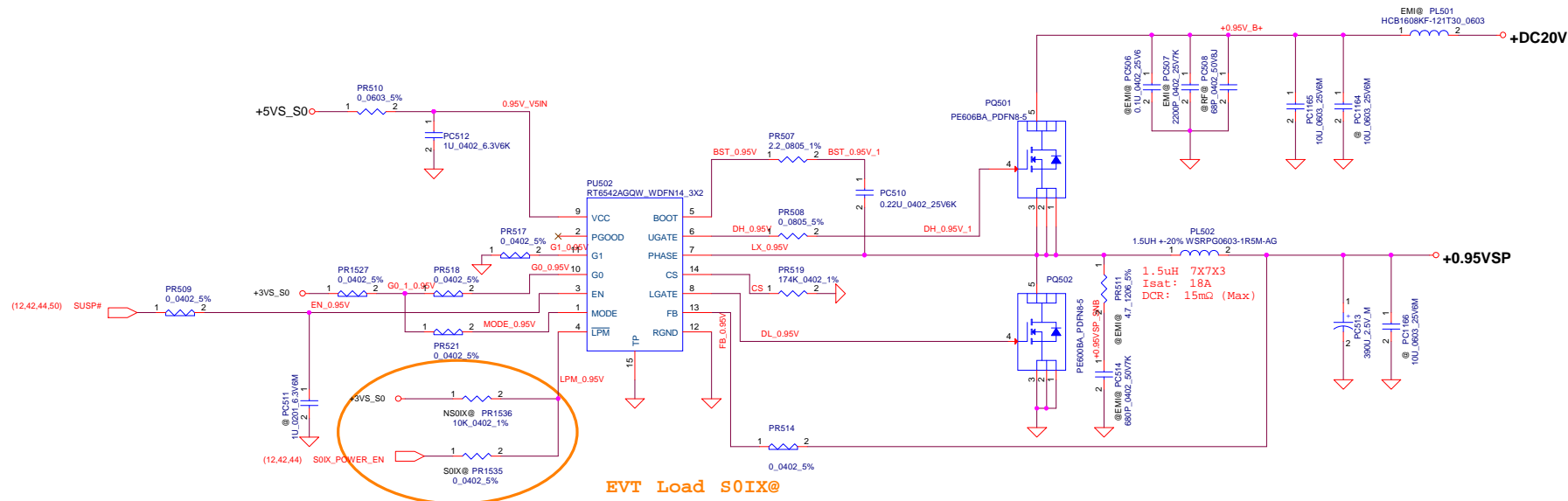
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2014/12/26	Deciphered Date	2017/10/19	Title	1.8V(RT8068A)	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev 0.1
				Date:	Tuesday, December 04, 2018	Sheet



+VPCH_1.05VP
Vin = 20V
Iin = 1.05*9.49/0.85/20
= 0.586A

Vout = Vfb*[1+(Rt/Rb)]
= 0.7*[1+(5K/10K)]
= 1.05V

+VPCH_1.05VP
Imax=6.65A, Ipeak=9.49A; Fsw=290K
Iocp=(Rcs1*Itrip)/Rdson
Rds : L/S --> typ:10.2mohm ; max: 14mohm
Itrip=9-11 uA
Iocp(set)=14-18
Iin_ripple= 1.58A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=1.559A
LIR=Delta IL/Ipeak=0.164
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=1355.25uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.57uF



EVT Load S0IX@

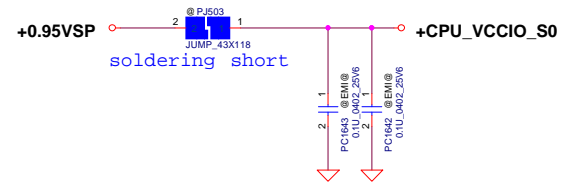
NS0IX@ for non-morden standby DVT EOC20 UMA Load S0IX@
DIS Load NS0IX@
EOY10 UMA Load S0IX@

PVT EOC20 UMA Load NS0IX@
DIS Load NS0IX@
EOY10 UMA Load S0IX@

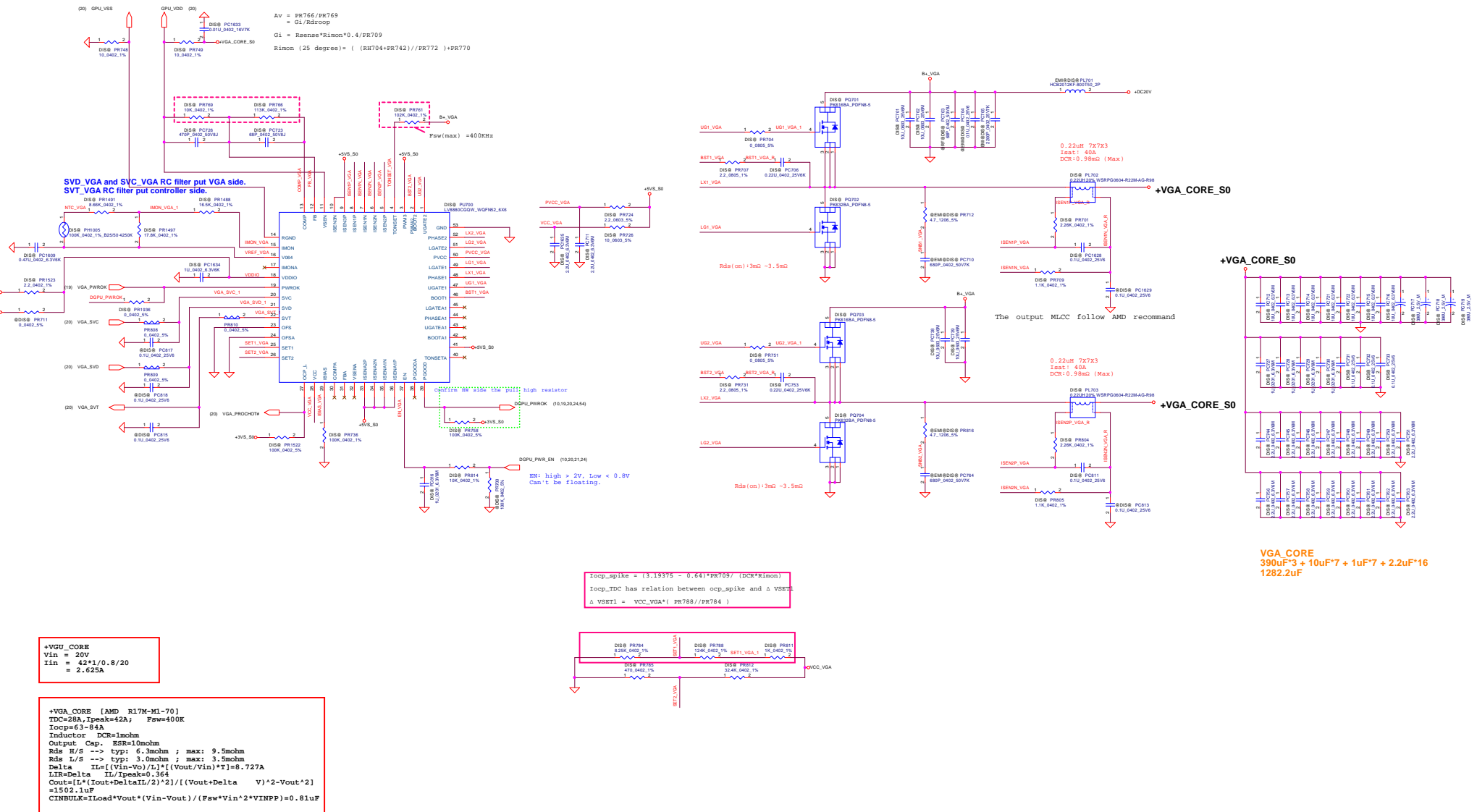
+0.95VSP
Vin = 20V
Iin = 0.95*5.95/0.85/20
= 0.3325A

VR	LPM	G1	G0	Vout
VCCIO	1	0	1	0.95V

+0.95VSP
Imax=4.165, Ipeak=5.95A; Fsw=290KHz
Iocp=(Rcs1*Itrip)/Rdson
Rds : L/S --> typ:10.2mohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=10~14A
Iin_ripple=2.04A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=2.08A
LIR=Delta IL/Ipeak=0.35
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=739.41uF
CINBULK=Iload*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.32uF

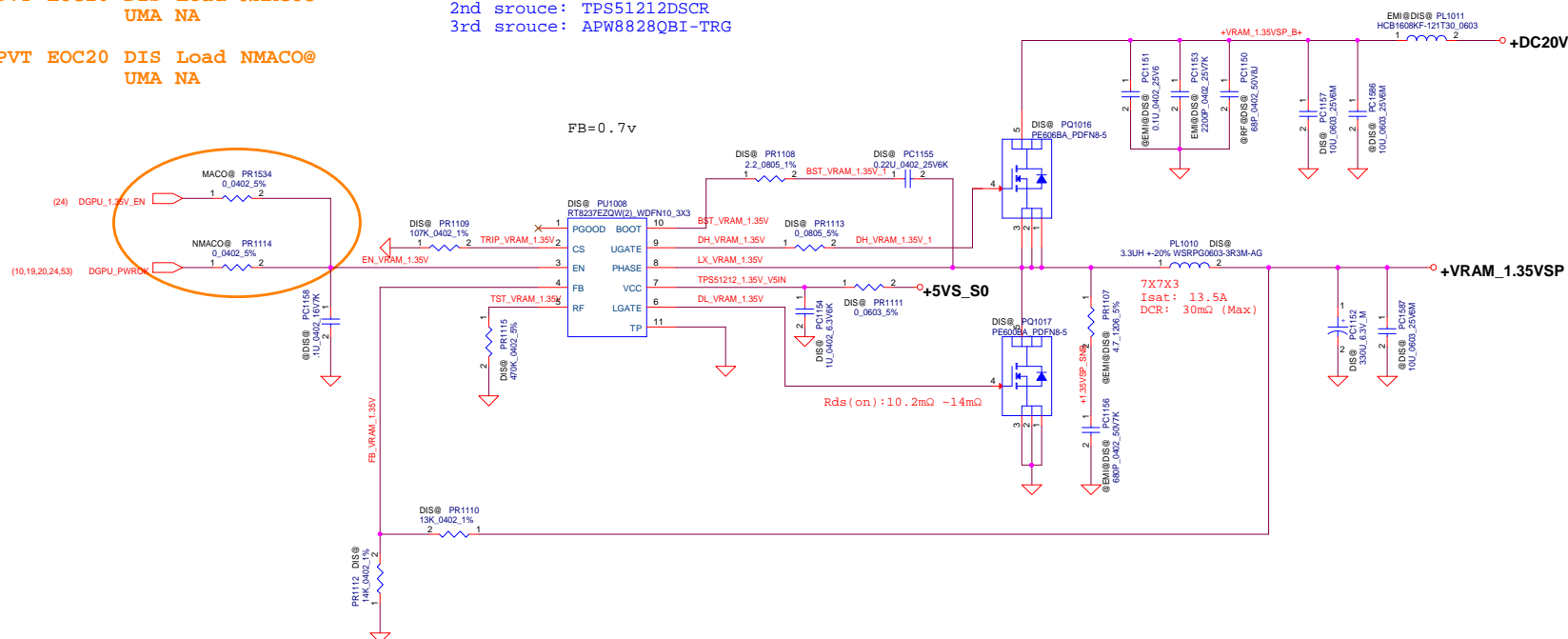


Security Classification		Compal Secret Data		Title	
Issued Date	2010/01/25	Deciphered Date	2017/10/19	Size	Document Number
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Rev	0.1
				Date:	Tuesday, December 04, 2018
				Sheet	52 of 63



PVT EOC20 DIS Load NMACO@
UMA NA

```
1st source: RT8237EZQW
2nd srouce: TPS51212DSCR
3rd srouce: APW8828QBI-TRG
```



```
+VRAM_1.35VSP
Vin = 20V
Iin = 1.35*3.82/0.85/20
     = 0.305A
```

$$\begin{aligned} V_{out} &= V_{fb} * [1 + (R_t / R_b)] \\ &= 0.7 * [1 + (13K / 14K)] \\ &= 1.35V \end{aligned}$$

```

+VRAM_1.35VSP
Imax=2.688A,Ipeak=3.84A      ;Fsw=290KHz
Iocp=(Rcs1*Itrip)/RdsOn
Rds : 1/S --> typ:10.1mohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=10~13.5A
Iin_ripple=0.53A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=1.272A
LIR=Delta IL/Ipeak=1.315
Coct=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=197.74uF
CINBULK=Lload*Iout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.29uF

```



Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date		2013/08/29	Deciphered Date		2013/08/29	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						VRAM 1.35V(RT8237EZQW)
						Size C
Date:				Tuesday, December 04, 2018		Sheet 54 of 63

CPU Type	BOM Structure
WHU-U42 (15W)	WHU-U42@
CML-Base (15W)	WHU-U42@
CML-Performance	CML@

WHU-U42 (15W)
 (A: TDC=4A, Ipeak=70A, Iloadline=1.8mohm
 GT: TDC=31A, Ipeak=31A, Iloadline=3.1mohm
 SA: TDC=4A, Ipeak=6A, Iloadline=10.3mohm

CML-Base (15W)
 (A: TDC=4A, Ipeak=70A, Iloadline=1.8mohm
 GT: TDC=31A, Ipeak=31A, Iloadline=3.1mohm
 SA: TDC=4A, Ipeak=6A, Iloadline=10.3mohm

CML-Performance (15W)
 (A: TDC=58A, Ipeak=85A, Iloadline=1.8mohm
 GT: TDC=18A, Ipeak=31A, Iloadline=3.1mohm
 SA: TDC=4A, Ipeak=6A, Iloadline=10.3mohm

WHU-U-LINE 42 15W

+CPU_CORE TDC=48A, Ipeak=70A Fsw=400K, OCP=84-119A Inductor DCR=0.9mohm Output Cap. ESR=10mohm Rds R/S --> typ: 6.3mohm ; maxi: 9.5mohm Rds L/S --> typ: 3.0mohm ; maxi: 3.5mohm Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=10.795A LIR=Delta IL/Ipeak=0.308 Cout=[L*(Iout-DeltaIL/2)^2]/[(Vout-Delta V)^2-Vout^2] =1518.56 CINSBULK=Iload*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.45uF	+GFX_CORE TDC=31A, Ipeak=31A Fsw=400K, OCP=40-53A Inductor DCR=0.9mohm Output Cap. ESR=10mohm Rds R/S --> typ: 6.3mohm ; maxi: 9.5mohm Rds L/S --> typ: 3.0mohm ; maxi: 3.5mohm Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=10.795A LIR=Delta IL/Ipeak=0.348 Cout=[L*(Iout-DeltaIL/2)^2]/[(Vout-Delta V)^2-Vout^2] =1576.0uF CINSBULK=Iload*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.29uF	+SA_CORE TDC=4A, Ipeak=6A Fsw=400K, OCP=12-24A Inductor DCR=4.2mohm Output Cap. ESR=10mohm Rds R/S --> typ: 19mohm ; maxi: 27mohm Rds L/S --> typ: 10.2mohm ; maxi: 14mohm Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=5.053A LIR=Delta IL/Ipeak=0.842 Cout=[L*(Iout-DeltaIL/2)^2]/[(Vout-Delta V)^2-Vout^2] =207.47uF CINSBULK=Iload*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.25uF
--	--	--

CML-U-LINE Base 15W

+CPU_CORE TDC=48A, Ipeak=70A Fsw=400K, OCP=84-119A Inductor DCR=0.9mohm Output Cap. ESR=10mohm Rds R/S --> typ: 6.3mohm ; maxi: 9.5mohm Rds L/S --> typ: 3.0mohm ; maxi: 3.5mohm Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=10.795A LIR=Delta IL/Ipeak=0.308 Cout=[L*(Iout-DeltaIL/2)^2]/[(Vout-Delta V)^2-Vout^2] =1518.56 CINSBULK=Iload*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.45uF	+GFX_CORE TDC=31A, Ipeak=31A Fsw=400K, OCP=40-53A Inductor DCR=0.9mohm Output Cap. ESR=10mohm Rds R/S --> typ: 6.3mohm ; maxi: 9.5mohm Rds L/S --> typ: 3.0mohm ; maxi: 3.5mohm Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=10.795A LIR=Delta IL/Ipeak=0.348 Cout=[L*(Iout-DeltaIL/2)^2]/[(Vout-Delta V)^2-Vout^2] =1576.0uF CINSBULK=Iload*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.29uF	+SA_CORE TDC=4A, Ipeak=6A Fsw=400K, OCP=12-24A Inductor DCR=4.2mohm Output Cap. ESR=10mohm Rds R/S --> typ: 19mohm ; maxi: 27mohm Rds L/S --> typ: 10.2mohm ; maxi: 14mohm Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=5.053A LIR=Delta IL/Ipeak=0.842 Cout=[L*(Iout-DeltaIL/2)^2]/[(Vout-Delta V)^2-Vout^2] =207.47uF CINSBULK=Iload*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.25uF
--	--	--

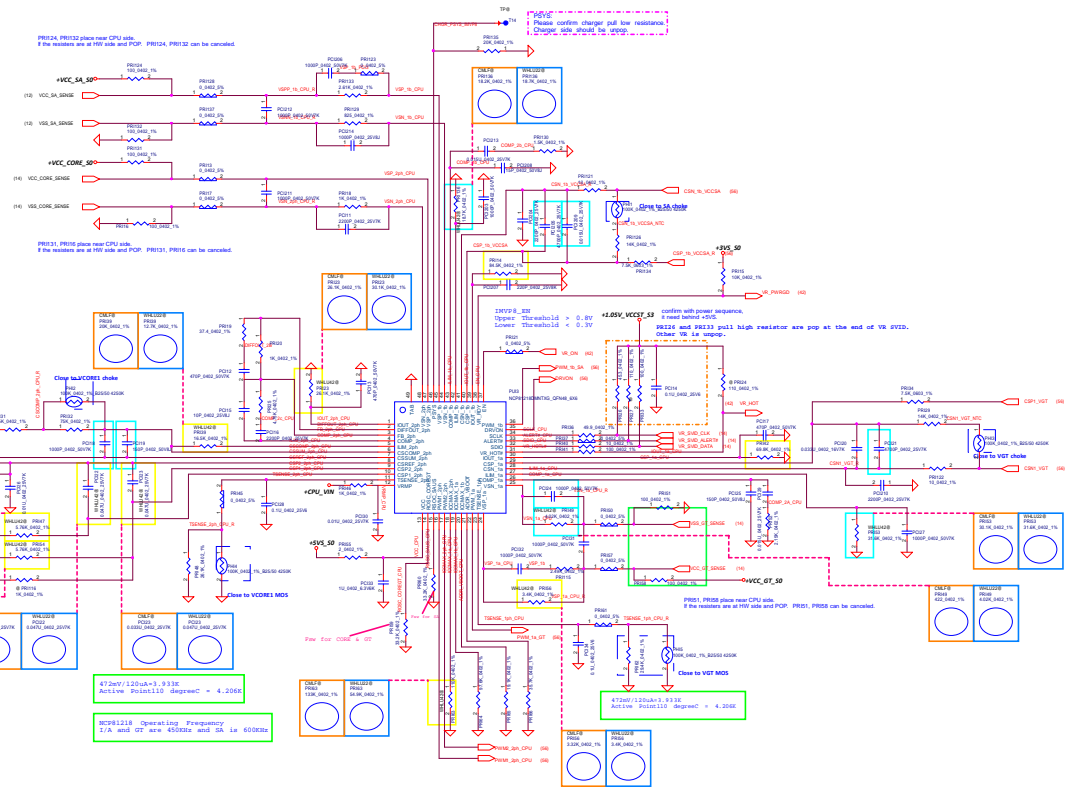
CML-U-LINE Performance 15W

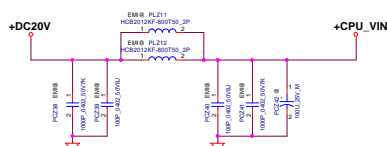
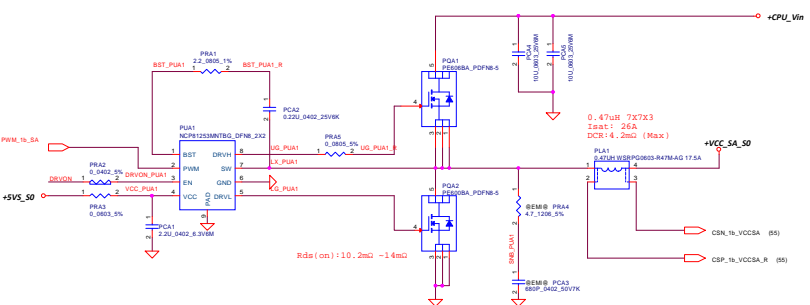
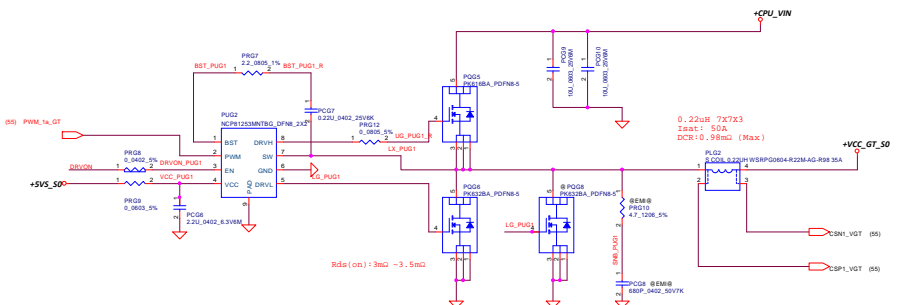
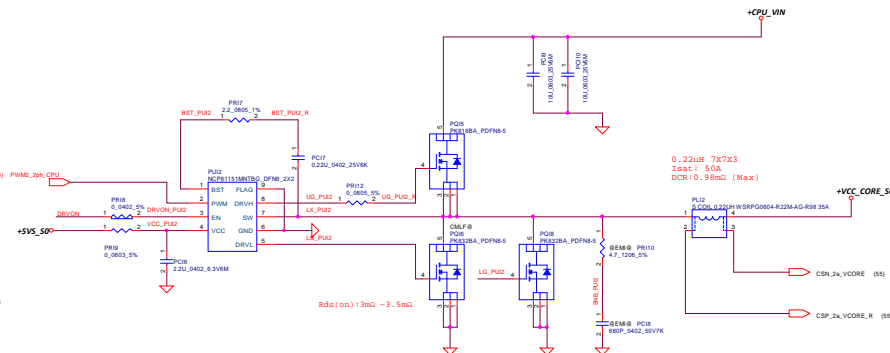
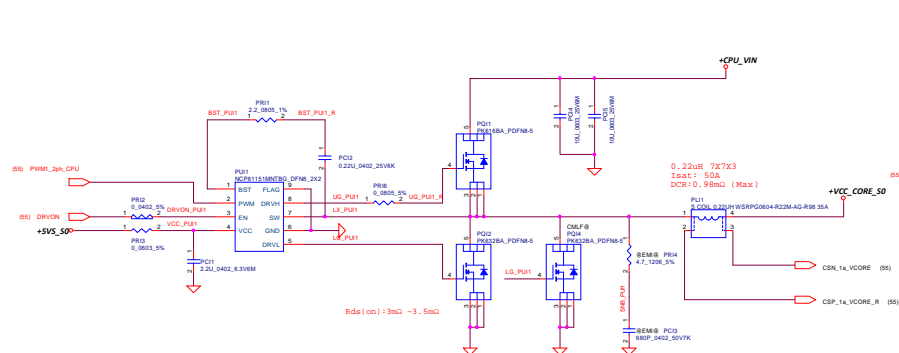
+CPU_CORE TDC=58A, Ipeak=85A Fsw=400K, OCP=TBD Inductor DCR=0.9mohm Output Cap. ESR=10mohm Rds R/S --> typ: 6.3mohm ; maxi: 9.5mohm Rds L/S --> typ: 3.0mohm ; maxi: 3.5mohm Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=10.795A LIR=Delta IL/Ipeak=0.308 Cout=[L*(Iout-DeltaIL/2)^2]/[(Vout-Delta V)^2-Vout^2] =1518.56 CINSBULK=Iload*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.45uF	+GFX_CORE TDC=31A, Ipeak=31A Fsw=400K, OCP=40-53A Inductor DCR=0.9mohm Output Cap. ESR=10mohm Rds R/S --> typ: 6.3mohm ; maxi: 9.5mohm Rds L/S --> typ: 3.0mohm ; maxi: 3.5mohm Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=10.795A LIR=Delta IL/Ipeak=0.348 Cout=[L*(Iout-DeltaIL/2)^2]/[(Vout-Delta V)^2-Vout^2] =1576.0uF CINSBULK=Iload*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.29uF	+SA_CORE TDC=4A, Ipeak=6A Fsw=400K, OCP=12-24A Inductor DCR=4.2mohm Output Cap. ESR=10mohm Rds R/S --> typ: 19mohm ; maxi: 27mohm Rds L/S --> typ: 10.2mohm ; maxi: 14mohm Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=5.053A LIR=Delta IL/Ipeak=0.842 Cout=[L*(Iout-DeltaIL/2)^2]/[(Vout-Delta V)^2-Vout^2] =207.47uF CINSBULK=Iload*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.25uF
--	--	--

U22: OCPWVOC= 40A
 RLIMWVOC=8.76E ->PR139
 U42: OCPWVOC= 70A ->PR139
 RLIMWVOC=16.9E ->PR139
 RLIM= IoutLIM*V Load Line/10
 U22: IoutMAXVOC= 32A ->PR123
 RLIMWVOC=64A ->PR123
 U42: IoutMAXVOC= 64A ->PR123
 RLIMWVOC=128A ->PR123
 RLIM= 2* RLIM /10 *IOUT1MAX * Load Line
 U22: Load LineWVOC= 2.4u
 RLIMWVOC=111E ->PR120
 U42: Load LineWVOC= 2.4u
 RLIMWVOC=111E ->PR130, PR138
 Load Line= (RDS1+RDS1*(RDS1+RDS1))
 *IOUT1MAX * VOUT/100

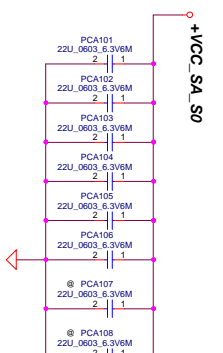
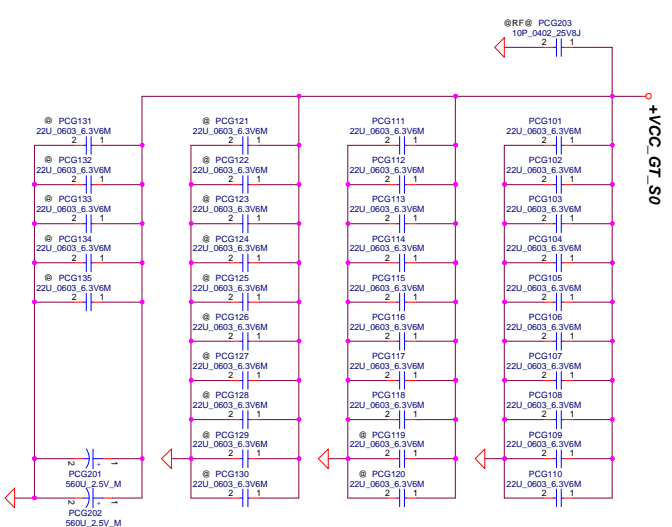
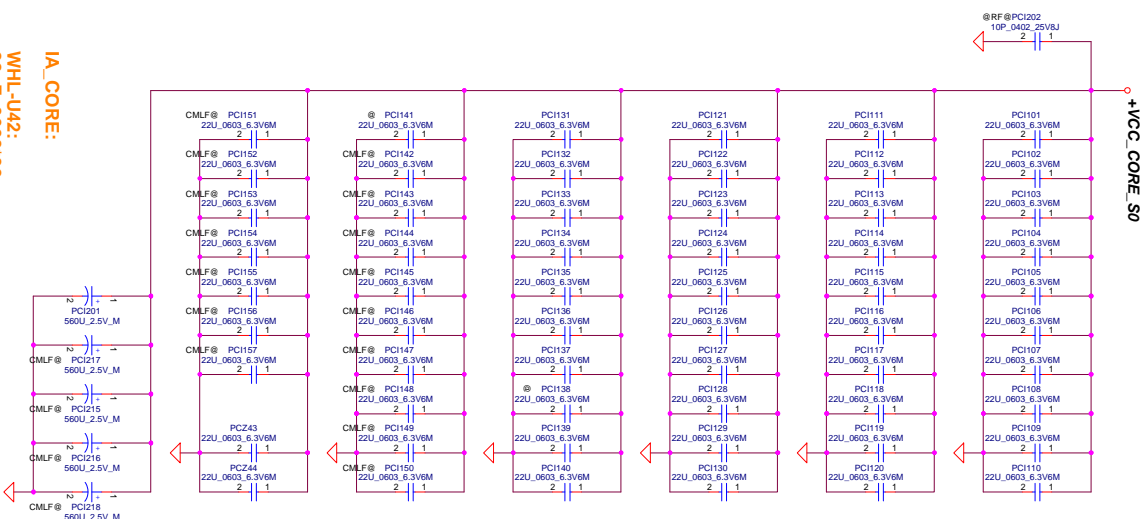
IS=MAXIS= 5A
 RLIMMAXIS= 15.8E ->PR165
 RLIMMAXIS=ISMAX*2V/10A/64A
 ISOUTMAX= 5A
 RLIMOUTMAX=49.8E ->PR114
 RLIMOUTMAX=ISMAX*2V/10A/64A
 ISMAX= 1.2V/(gm*(RDS1+RDS2)*IoutLIM*VOC
 / (RDS1+RDS1+RDS2))
 OCPW= 9.5A ->PR25
 RLIMW=1.2V/(gm*(RDS1+RDS2)*IoutLIM*VOC
 / (RDS1+RDS1+RDS2))
 ISMAX=10.3u
 RLIMMAX=1.2E ->PR14
 RLIMW= Load Line*(RDS1+RDS2)*IoutLIM*VOC
 / (gm * VOUT) / (RDS1+RDS2))

U22/U42: Load LineWVOC= 3.1m
 RLIMWVOC=8.76E ->PR136
 RLIMWVOC=ISMAX*2V/10A/64A
 U22: IoutMAXVOC= 31A ->PR164
 RLIMWVOC= 97.6E ->PR164
 U42: IoutMAXVOC= 31A ->PR164
 RLIMWVOC= 97.6E ->PR164
 RLIMWVOC=ISMAX*2V/10A/64A
 U22: IOUT1MAXVOC= 31A ->PR162
 RLIMWVOC= 97.6E ->PR162
 U42: IOUT1MAXVOC= 31A ->PR162
 RLIMWVOC= 97.6E ->PR162
 RLIMWVOC=ISMAX*2V/10A/64A
 OCPW= 30A
 RLIMWVOC=29.4E ->PR153
 RLIMWVOC=ISMAX*2V/10A/64A
 RLIMWVOC=ISMAX*2V/10A/64A





Security Classification		Compul Secret Data		Compul Electronics, Inc.	
Issued Date		Designed Date		Yes	
		2016/10/2		CPU_CORE(PowerStage)	
THE SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMFUL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE REPRODUCED, COPIED, OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, WITHOUT THE WRITTEN CONSENT OF COMFUL ELECTRONICS, INC.		Size		Rev	
		1		0.1	
Date		Tuesday, November 04, 2016		Sheet 55 of 83	



IA_CORE:
WHL-U42:
22uF_0603*39
560uF_10m*1

CML_Base:
22uF_0603*39
560uF_10m*1

CML_Performance:
22uF_0603*45
560uF_10m*5

```
GT_CORE
WHL-U42:
22uF_0603*18
560uF_10m*2

CML-Base:
22uF_0603*18
560uF_10m*2

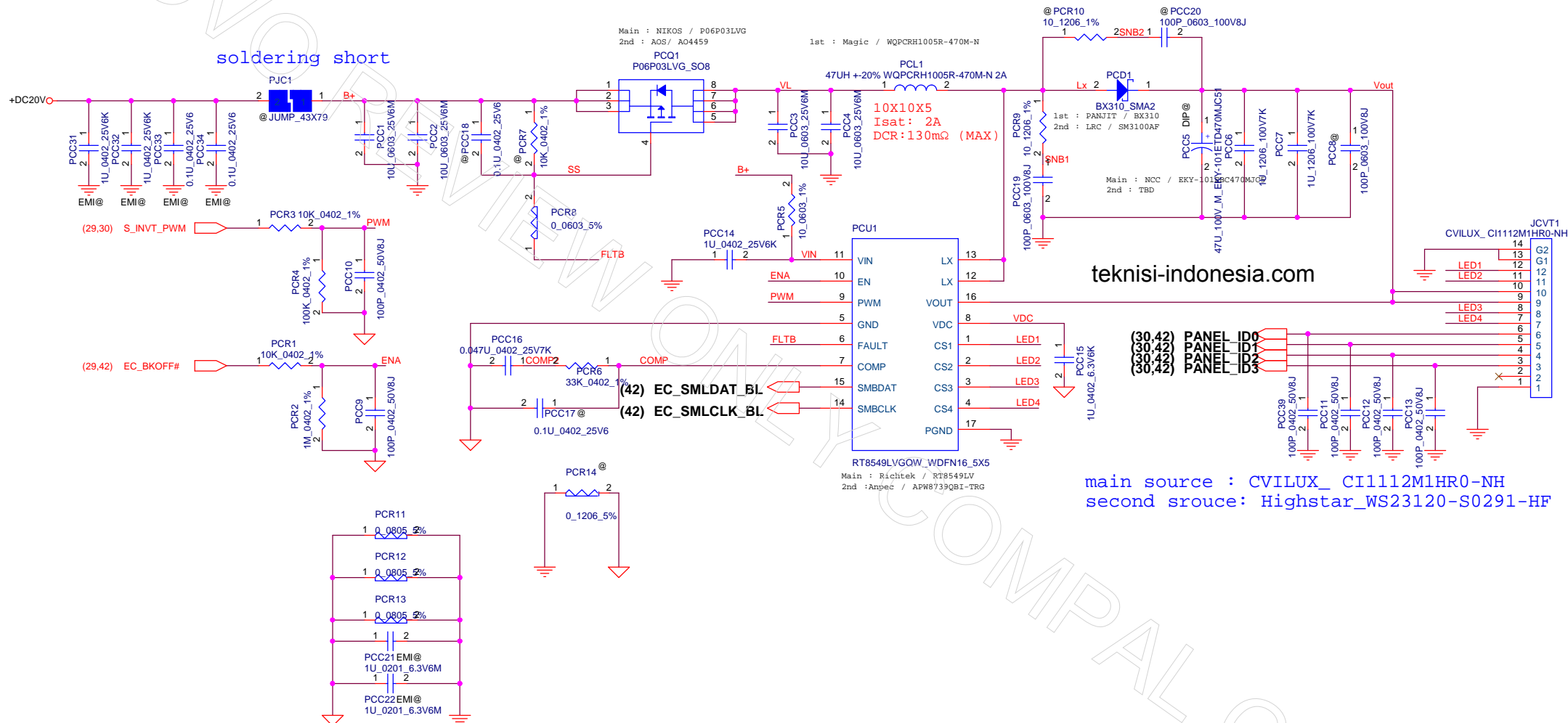
CML-Performance:
22uF_0603*18
560uF_10m*2
```

SA_CORE
WHL-U42:
22uF_0603*6
CML-Base:
22uF_0603*6
CML-Performance
22uF_0603*6

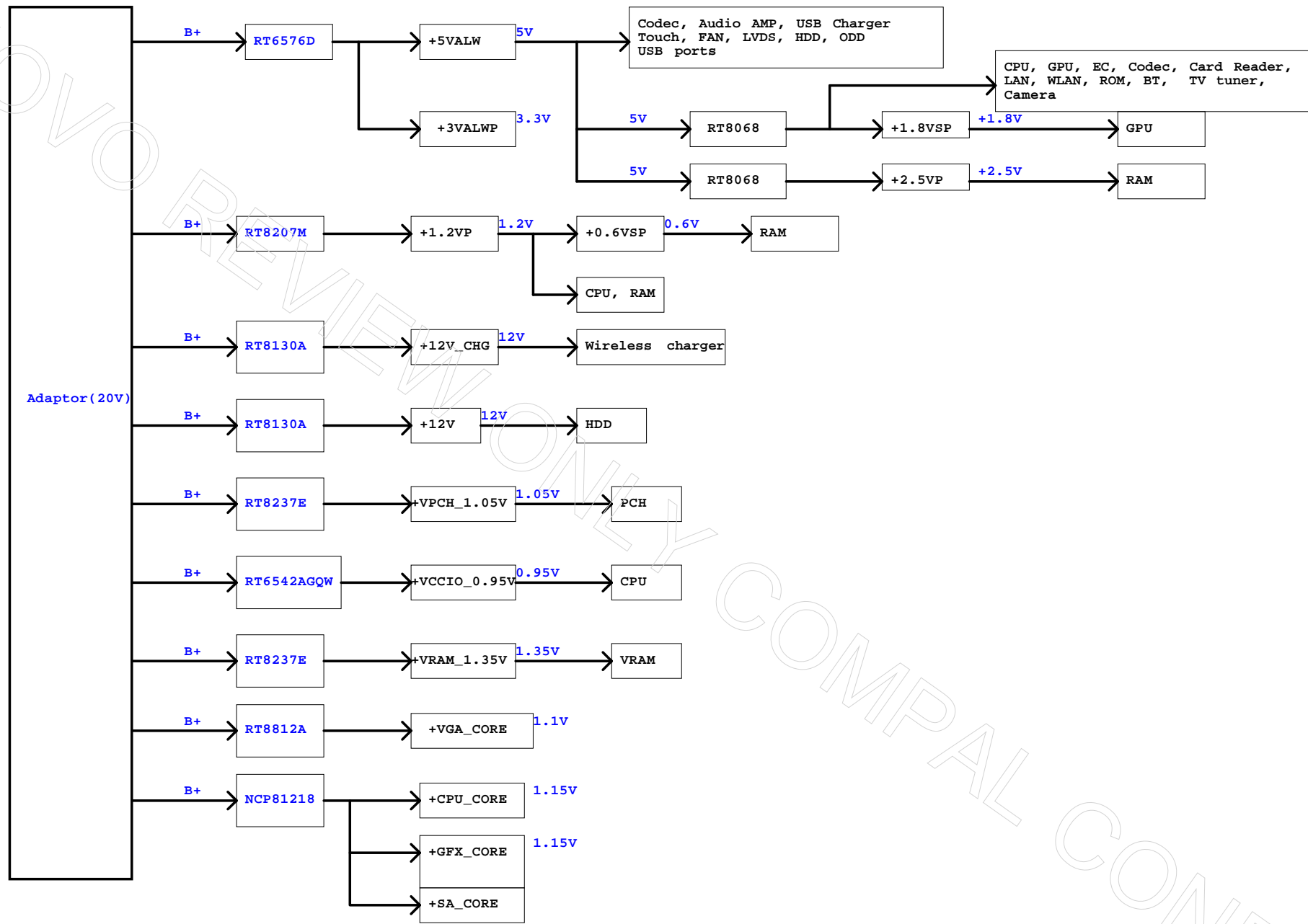
Security Classification		Compil Secret Data		This	
Issued Date		Declassified Date	2016/1/22		
THIS SET OF INFORMATION IS THE PROTECTIVE PROPERTY OF COMPAQ ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS TO BE KEPT SECRET AND NOT DISCLOSED TO ANY OTHER PERSON OR ORGANIZATION WITHOUT THE WRITTEN PERMISSION OF COMPAQ ELECTRONICS, INC. WITHOUT SUCH PERMISSION, NO PART OF THIS INFORMATION IS TO BE REPRODUCED, COPIED, OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM.					
Date		Serial		Page	
1987		57		63	

This is GND_POWER

soldering short



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/11/25	Deciphered Date	2015/11/25	Title	CONVERTER/B
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size B	Document Number
				Date:	Rev 0.1
				LA-D952P M/B	
				Sheet	58 of 63



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/12/18	Deciphered Date	2013/12/18	Title Power Rail	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Rev 0.1
				Date: Tuesday, December 04, 2018	Sheet 59 of 63

366439_CNL_PCH_U_EDS_Vol_1_Rev_1.1				ECCD_061(WHL)	
Group	Sail	GPIO Number	GPIO Name	Signal name	External PU/PD
GPIO	BV36	GPIO0	BATLOW#	PM_BATLOW#	PU 8.2K to +3VALW_SS
	BV35	GPIO1	ACPRESENT#	AC_PRESENT#	PU 10K to +3VALW_SS (B)
	BV32	GPIO2	LAN_WAKE#	LAN_WAKE#	NC
	BV28	GPIO3	PAINTEN#	PAINTEN#	TP
	BV36	GPIO4	SUP_55#	PM_SUP_55#	PU 10K to +3VALW_SS
	BV27	GPIO5	SUP_54#	PM_SUP_54#	PU 10K to +3VALW_SS
	BV37	GPIO6	SUP_4#	NC	NC
	BV35	GPIO7	GPD_7	SOC_GPD7	PU 100K to +3VALW_SS
	BV32	GPIO8	SUSCLK	SUSCLK	NC
	BV30	GPIO9	WAKEUP#	NC	NC
GPIO	BV29	GPIO10	SUP_55#	PM_SUP_55#	TP
	BV34	GPIO11	LAN PHY PC	NC	NC
	BV28	GPIO_A0	ECIM	KB_RST#	PU 10K to +3V5_50
	CA29	GPIO_A1	TIME_SYNC1	LPC_A00	LPC_A00
	BV29	GPIO_A2	LAD1	LPC_A01	LPC_A01
	BV27	GPIO_A3	LAD2	LPC_A02	LPC_A02
	BV27	GPIO_A4	LAD3	LPC_A03	LPC_A03
	CA28	GPIO_A5	LPC_FRAME#	LPC_FRAME#	NC
	BV28	GPIO_A6	SERIRQ	SERIRQ	PU 8.2K to +3V5_50
	CC32	GPIO_A7	FIRQA#	SOC_GPP_A7	PU 10K to +3V5_50
GPIO	BV30	GPIO_A8	CLURUN#	PM_CLKRUN#	PU 8.2K to +3V5_50
	BV32	GPIO_A9	CLURUN#	LPC_CLK0	NC
	BV30	GPIO_A10	PLWEN	NC	NC
	CA32	GPIO_A11	GPIO1_CS1#	NC	NC
	BV37	GPIO_A12	BW_BW_SW	ISN_GPD6/55_EXIT_H_CLODFF#	NC
	BV34	GPIO_A13	SUSWARM	SUSWARM	NC
	CA27	GPIO_A14	SUSWARM	ESPI_RESET#	WL_ON
	BV32	GPIO_A15	SUSACK#	SUSACK#	NC
	BV31	GPIO_A16	SD_IP0_SEL	NC	NC
	BV36	GPIO_A17	SD_VDD1_PWR_EN#	ISN_GPD7	NC
GPIO	BV35	GPIO_A18	ISN_GPD0	NC	NC
	BV34	GPIO_A19	ISN_GPD1	NC	NC
	CA37	GPIO_A20	ISN_GPD2	NC	NC
	CA36	GPIO_A21	ISN_GPD3	NC	NC
	CA35	GPIO_A22	ISN_GPD4	NC	NC
	CA34	GPIO_A23	ISN_GPD5	NC	NC
	CB36	GPIO_B0	NC	NC	NC
	CB35	GPIO_B1	NC	NC	NC
	CC36	GPIO_B2	VREALERT#	SOC_VREALERT#	PU 10K to +3VALW_SS (B)
	CB34	GPIO_B3	CVU_DP2	NC	NC
GPIO	CC35	GPIO_B4	CVU_DP3	NC	NC
	CF32	GPIO_B5	SRCLKREQ0#	CLKREQ_V0AM	PU 10K to +3V5_50
	CE32	GPIO_B6	SRCLKREQ01#	CLKREQ_L0AM	PU 10K to +3V5_50
	CF30	GPIO_B7	SRCLKREQ03#	CLKREQ_W0AM	PU 10K to +3V5_50
	CE31	GPIO_B8	SRCLKREQ03#	NC	NC
	CE30	GPIO_B9	SRCLKREQ04#	CLKREQ_S0H	PU 10K to +3V5_50
	CF31	GPIO_B10	SRCLKREQ03#	NC	NC
	CC37	GPIO_B11	EXT_PCH0_GATE#	NC	NC
	BV37	GPIO_B12	SUP_50#	PM_SUP_50#	PU 10K to +3V5_50
	BV35	GPIO_B13	PLTRST#	SOC_PLTRST#	NC
GPIO	CF35	GPIO_B14	SPKR	HDA_SPKR	PU 2.2K to +3V5_50 (B)
	CC27	GPIO_B15	GPIO_CS0#	NC	NC
	CE28	GPIO_B16	GPIO_CS0#	GPIO_B16	TP
	CC27	GPIO_B17	GPIO_MISO	NC	NC
	CE29	GPIO_B18	GPIO_MOSI	GPIO_MOSI	NC
	CA31	GPIO_B19	GPIO_CS0#	NC	NC
	CC29	GPIO_B20	GPIO_CS0#	NC	NC
	CC30	GPIO_B21	GPIO_MISO	NC	NC
	CA30	GPIO_B22	GPIO_MOSI	GPIO_MOSI	NC
	CC34	GPIO_B23	SMLALERT#	SOC_SMLALERT#	NC
GPIO	CK14	GPIO_C0	SMBCLK	PM_SMBCLK	PU 2.2K to +3VALW_SS
	CK15	GPIO_C1	SMBDATA	PM_SMBDATA	PU 2.2K to +3VALW_SS
	CK15	GPIO_C2	SMBALERT#	SOC_SMBALERT#	NC
	CK14	GPIO_C3	SMLCLK	SOC_SMLCLK	PU 1K to +3V5_50
	CK15	GPIO_C4	SMLDATA	SOC_SMLDATA	PU 1K to +3V5_50
	CK15	GPIO_C5	SMLALERT#	SOC_SMLALERT#	NC
	CK15	GPIO_C6	SMLCLK	EC_SMB_CLK	PU 1K to +3V5_50
	CK14	GPIO_C7	SMLDATA	EC_SMB_DATA	PU 1K to +3V5_50
	CK14	GPIO_C8	UART0_RXD	NC	NC
	CK14	GPIO_C9	UART0_TXD	NC	NC
GPIO	CK14	GPIO_C10	UART0_RTS#	NC	NC
	CK14	GPIO_C11	UART0_CTS#	BT_ON	PU 10K to +3V5_50 (B)
	CK12	GPIO_C12	UART1_RXD	DGPP_UART1_RXD	PU 10K to +3V5_50 (B)
	CK12	GPIO_C13	UART1_TXD	DGPP_HOLD_RST#	PU 10K to +3V5_50 (B)
	CK12	GPIO_C14	UART1_RTS#	DGPP_PWRON	PU 100K to +3V5_50 (B)
	CK14	GPIO_C15	UART1_CTS#	DGPP_PRTN#	PU 10K to +3V5_50 (B)
	CK11	GPIO_C16	I2C0_SDA	NC	NC
	CK11	GPIO_C17	I2C0_SCL	NC	NC
	CK12	GPIO_C18	I2C1_SDA	NC	NC
	CK12	GPIO_C19	I2C1_SCL	NC	NC
GPIO	CK12	GPIO_C20	UART2_RXD	NC	NC
	CK12	GPIO_C21	UART2_TXD	NC	NC
	CK12	GPIO_C22	UART2_RTS#	NC	NC
	CK12	GPIO_C23	UART2_CTS#	NC	NC
	CK12	GPIO_C24	UART2_CTS#	NC	NC
	CK12	GPIO_C25	UART2_CTS#	NC	NC
	CK12	GPIO_C26	UART2_CTS#	NC	NC
	CK12	GPIO_C27	UART2_CTS#	NC	NC
	CK12	GPIO_C28	UART2_CTS#	NC	NC
	CK12	GPIO_C29	UART2_CTS#	NC	NC
GPIO	CK12	GPIO_C30	UART2_CTS#	NC	NC
	CK12	GPIO_C31	UART2_CTS#	NC	NC
	CK12	GPIO_C32	UART2_CTS#	NC	NC
	CK12	GPIO_C33	UART2_CTS#	NC	NC
	CK12	GPIO_C34	UART2_CTS#	NC	NC
	CK12	GPIO_C35	UART2_CTS#	NC	NC
	CK12	GPIO_C36	UART2_CTS#	NC	NC
	CK12	GPIO_C37	UART2_CTS#	NC	NC
	CK12	GPIO_C38	UART2_CTS#	NC	NC
	CK12	GPIO_C39	UART2_CTS#	NC	NC
GPIO	CK12	GPIO_C40	UART2_CTS#	NC	NC
	CK12	GPIO_C41	UART2_CTS#	NC	NC
	CK12	GPIO_C42	UART2_CTS#	NC	NC
	CK12	GPIO_C43	UART2_CTS#	NC	NC
	CK12	GPIO_C44	UART2_CTS#	NC	NC
	CK12	GPIO_C45	UART2_CTS#	NC	NC
	CK12	GPIO_C46	UART2_CTS#	NC	NC
	CK12	GPIO_C47	UART2_CTS#	NC	NC
	CK12	GPIO_C48	UART2_CTS#	NC	NC
	CK12	GPIO_C49	UART2_CTS#	NC	NC
GPIO	CK12	GPIO_C50	UART2_CTS#	NC	NC
	CK12	GPIO_C51	UART2_CTS#	NC	NC
	CK12	GPIO_C52	UART2_CTS#	NC	NC
	CK12	GPIO_C53	UART2_CTS#	NC	NC
	CK12	GPIO_C54	UART2_CTS#	NC	NC
	CK12	GPIO_C55	UART2_CTS#	NC	NC
	CK12	GPIO_C56	UART2_CTS#	NC	NC
	CK12	GPIO_C57	UART2_CTS#	NC	NC
	CK12	GPIO_C58	UART2_CTS#	NC	NC
	CK12	GPIO_C59	UART2_CTS#	NC	NC
GPIO	CK12	GPIO_C60	UART2_CTS#	NC	NC
	CK12	GPIO_C61	UART2_CTS#	NC	NC
	CK12	GPIO_C62	UART2_CTS#	NC	NC
	CK12	GPIO_C63	UART2_CTS#	NC	NC
	CK12	GPIO_C64	UART2_CTS#	NC	NC
	CK12	GPIO_C65	UART2_CTS#	NC	NC
	CK12	GPIO_C66	UART2_CTS#	NC	NC
	CK12	GPIO_C67	UART2_CTS#	NC	NC
	CK12	GPIO_C68	UART2_CTS#	NC	NC
	CK12	GPIO_C69	UART2_CTS#	NC	NC
GPIO	CK12	GPIO_C70	UART2_CTS#	NC	NC
	CK12	GPIO_C71	UART2_CTS#	NC	NC
	CK12	GPIO_C72	UART2_CTS#	NC	NC
	CK12	GPIO_C73	UART2_CTS#	NC	NC
	CK12	GPIO_C74	UART2_CTS#	NC	NC
	CK12	GPIO_C75	UART2_CTS#	NC	NC
	CK12	GPIO_C76	UART2_CTS#	NC	NC
	CK12	GPIO_C77	UART2_CTS#	NC	NC
	CK12	GPIO_C78	UART2_CTS#	NC	NC
	CK12	GPIO_C79	UART2_CTS#	NC	NC
GPIO	CK12	GPIO_C80	UART2_CTS#	NC	NC
	CK12	GPIO_C81	UART2_CTS#	NC	NC
	CK12	GPIO_C82	UART2_CTS#	NC	NC
	CK12	GPIO_C83	UART2_CTS#	NC	NC
	CK12	GPIO_C84	UART2_CTS#	NC	NC
	CK12	GPIO_C85	UART2_CTS#	NC	NC
	CK12	GPIO_C86	UART2_CTS#	NC	NC
	CK12	GPIO_C87	UART2_CTS#	NC	NC
	CK12	GPIO_C88	UART2_CTS#	NC	NC
	CK12	GPIO_C89	UART2_CTS#	NC	NC
GPIO	CK12	GPIO_C90	UART2_CTS#	NC	NC
	CK12	GPIO_C91	UART2_CTS#	NC	NC
	CK12	GPIO_C92	UART2_CTS#	NC	NC
	CK12	GPIO_C93	UART2_CTS#	NC	NC
	CK12	GPIO_C94	UART2_CTS#	NC	NC
	CK12	GPIO_C95	UART2_CTS#	NC	NC
	CK12	GPIO_C96	UART2_CTS#	NC	NC
	CK12	GPIO_C97	UART2_CTS#	NC	NC
	CK12	GPIO_C98	UART2_CTS#	NC	NC
	CK12	GPIO_C99	UART2_CTS#	NC	NC
GPIO	CK12	GPIO_C100	UART2_CTS#	NC	NC
	CK12	GPIO_C101	UART2_CTS#	NC	NC
	CK12	GPIO_C102	UART2_CTS#	NC	NC
	CK12	GPIO_C103	UART2_CTS#	NC	NC
	CK12	GPIO_C104	UART2_CTS#	NC	NC
	CK12	GPIO_C105	UART2_CTS#	NC	NC
	CK12	GPIO_C106	UART2_CTS#	NC	NC
	CK12	GPIO_C107	UART2_CTS#	NC	NC
	CK12	GPIO_C108	UART2_CTS#	NC	NC
	CK12	GPIO_C109	UART2_CTS#	NC	NC
GPIO	CK12	GPIO_C110	UART2_CTS#	NC	NC
	CK12	GPIO_C111	UART2_CTS#	NC	NC
	CK12	GPIO_C112	UART2_CTS#	NC	NC
	CK12	GPIO_C113	UART2_CTS#	NC	NC
	CK12	GPIO_C114	UART2_CTS#	NC	NC
	CK12	GPIO_C115	UART2_CTS#	NC	NC
	CK12	GPIO_C116	UART2_CTS#	NC	NC
	CK12	GPIO_C117	UART2_CTS#	NC	NC
	CK12	GPIO_C118	UART2_CTS#	NC	NC
	CK12	GPIO_C119	UART2_CTS#	NC	NC
GPIO	CK12	GPIO_C120	UART2_CTS#	NC	NC
	CK12	GPIO_C121	UART2_CTS#	NC	NC
	CK12	GPIO_C122	UART2_CTS#	NC	NC
	CK12	GPIO_C123	UART2_CTS#	NC	NC
	CK12	GPIO_C124	UART2_CTS#	NC	NC
	CK12	GPIO_C125	UART2_CTS#	NC	NC
	CK12	GPIO_C126	UART2_CTS#	NC	NC
	CK12	GPIO_C127	UART2_CTS#	NC	NC
	CK12	GPIO_C128	UART2_CTS#	NC	NC
	CK12	GPIO_C129	UART2_CTS#	NC	NC
GPIO	CK12	GPIO_C130	UART2_CTS#	NC	NC
	CK12	GPIO_C131	UART2_CTS#	NC	NC
	CK12	GPIO_C132	UART2_CTS#	NC	NC
	CK12	GPIO_C133	UART2_CTS#	NC	NC
	CK12	GPIO_C134	UART2_CTS#	NC	NC
	CK12	GPIO_C135	UART2_CTS#	NC	NC
	CK12	GPIO_C136	UART2_CTS#	NC	NC
	CK12	GPIO_C137	UART2_CTS#	NC	NC
	CK12	GPIO_C138	UART2_CTS#	NC	NC
	CK12	GPIO_C139	UART2_CTS#	NC	NC
GPIO	CK12	GPIO_C140	UART2_CTS#	NC	NC
	CK12	GPIO_C141	UART2_CTS#	NC	NC
	CK12	GPIO_C142	UART2_CTS#	NC	NC
	CK12	GPIO_C143	UART2_CTS#	NC	NC
	CK12	GPIO_C144	UART2_CTS#	NC	NC
	CK12	GPIO_C145	UART2_CTS#	NC	NC
	CK12	GPIO_C146	UART2_CTS#	NC	NC
	CK12	GPIO_C147	UART2_CTS#	NC	NC
	CK12	GPIO_C148	UART2_CTS#	NC	NC
	CK12	GPIO_C149	UART2_CTS#	NC	NC
GPIO	CK12	GPIO_C150	UART2_CTS#	NC	NC
	CK12	GPIO_C151	UART2_CTS#	NC	NC
	CK12	GPIO_C152	UART2_CTS#	NC	NC
	CK12	GPIO_C153	UART2_CTS#	NC	NC
	CK12	GPIO_C154	UART2_CTS#	NC	NC
	CK12	GPIO_C155	UART2_CTS#	NC	NC
	CK12	GPIO_C156	UART2_CTS#	NC	NC
	CK12	GPIO_C157	UART2_CTS#	NC	NC
	CK12	GPIO_C158	UART2_CTS#	NC	NC
	CK12	GPIO_C159	UART2_CTS#	NC	NC
GPIO	CK12	GPIO_C160	UART2_CTS#	NC	NC
	CK12	GPIO_C161	UART2_CTS#	NC	NC
	CK12	GPIO_C162	UART2_CTS#	NC	NC
	CK12	GPIO_C163	UART2_CTS#	NC	NC
	CK12	GPIO_C164	UART2_CTS#	NC	NC
	CK12	GPIO_C165	UART2_CTS#	NC	NC
	CK12	GPIO_C166	UART2_CTS#	NC	NC

